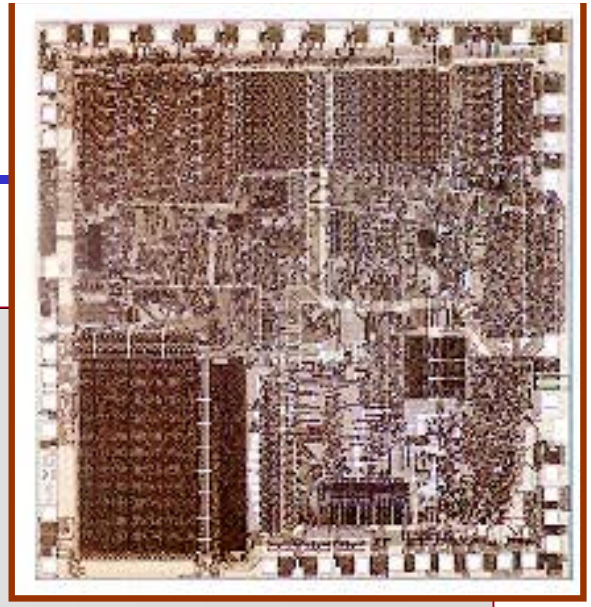
Week 8

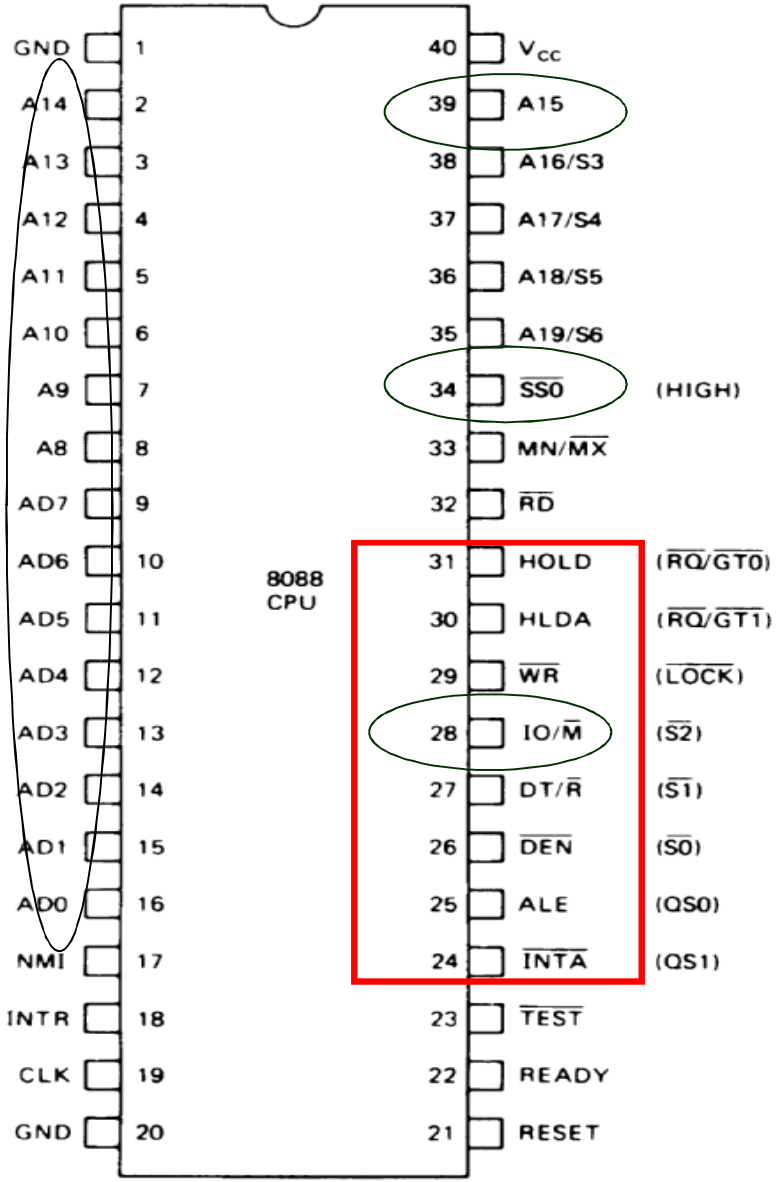
The 8088 and 8086 Microprocessors

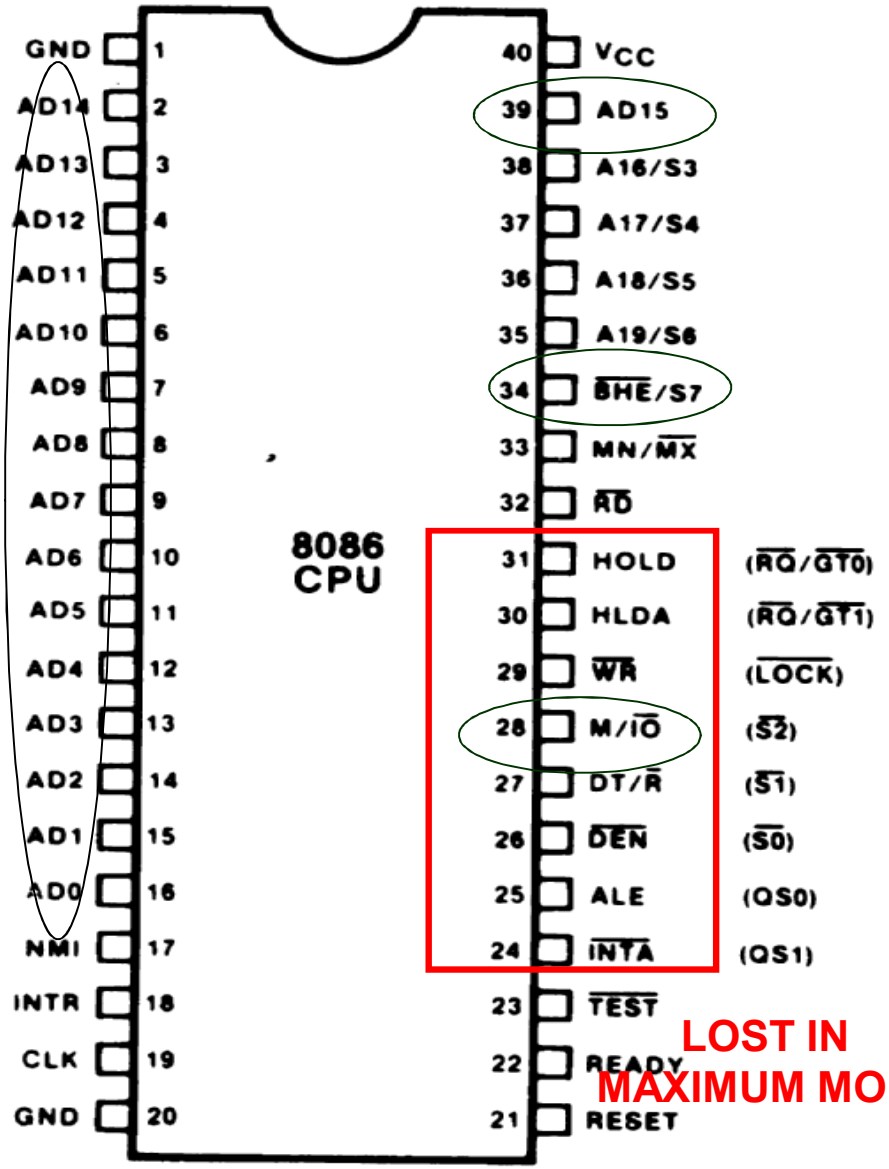
8086 and 8088 Microprocessors



- 8086 announced in 1978; 8086 is a 16 bit microprocessor with a 16 bit data bus
- 8088 announced in 1979; 8088 is a 16 bit microprocessor with an 8 bit data bus
- Both manufactured using High-performance Metal Oxide Semiconductor (HMOS) technology
- Both contain about 29000 transistors
- Both are packaged in 40 pin dual-in-line package (DIP)
- Address lines A0-A7 and Data lines D0-D7 are multiplexed in 8088. These lines are labelled as AD0-AD7.
  - By multiplexed we mean that the same pysical pin carries an address bit at one time and the data bit another time
- Address lines A0-A15 and Data lines D0-D15 are multiplexed in 8086. These lines are labelled as AD0-AD15.

8088 and 8086 Microprocessors





LOST IN MAXIMUM MODE

Minimum-mode and Maximum-mode Systems

- 8088 and 8086 microprocessors can be configured to work in either of the two modes: the minimum mode and the maximum mode

✓ Minimum mode:

- Pull MN/$\overline{MX}$ to logic 1
- Typically smaller systems and contains a single microprocessor
- Cheaper since all control signals for memory and I/O are generated by the microprocessor.

✓ Maximum mode

- Pull MN/**$\overline{MX}$** logic 0
- Larger systems with more than one processor (*designed to be used when a coprocessor (8087) exists in the system)*

PINs on microprocessor

Signals common to both minimum and maximum systems→

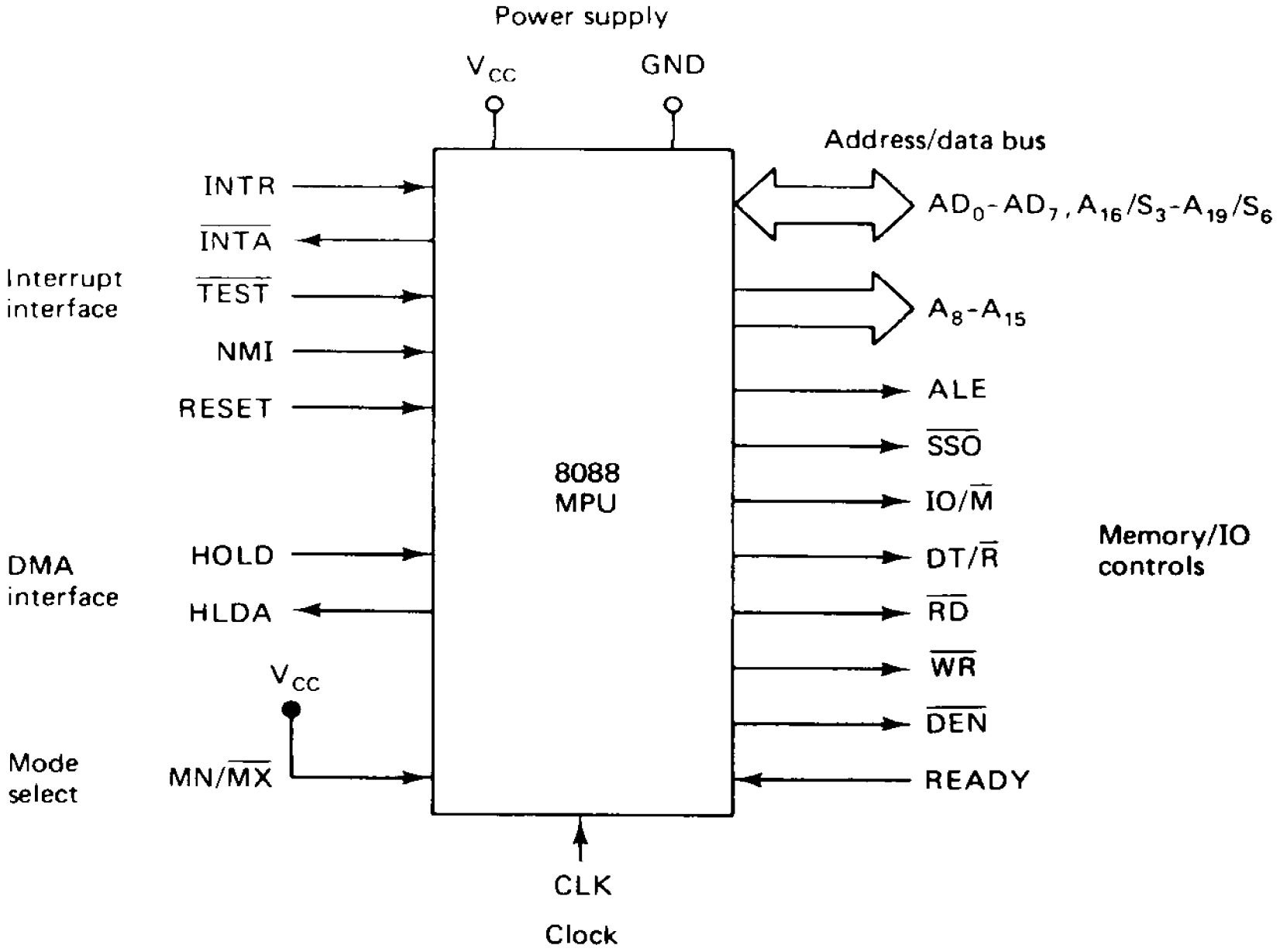
Common signals		
Name	**Function**	**Type**
AD7–AD0	Address/data bus	Bidirectional, 3-state
A15–A8	Address bus	Output, 3-state
A19/S6–A16/S3	Address/status	Output, 3-state
MN/$\overline{MX}$	Minimum/maximum Mode control	Input
$\overline{RD}$	Read control	Output, 3-state
$\overline{TEST}$	Wait on test control	Input
READY	Wait state control	Input
RESET	System reset	Input
NMI	Nonmaskable interrupt request	Input
INTR	Interrupt request	Input
CLK	System clock	Input
V_{cc}	+5 V	Input
GND	Ground	

PINs on microprocessor

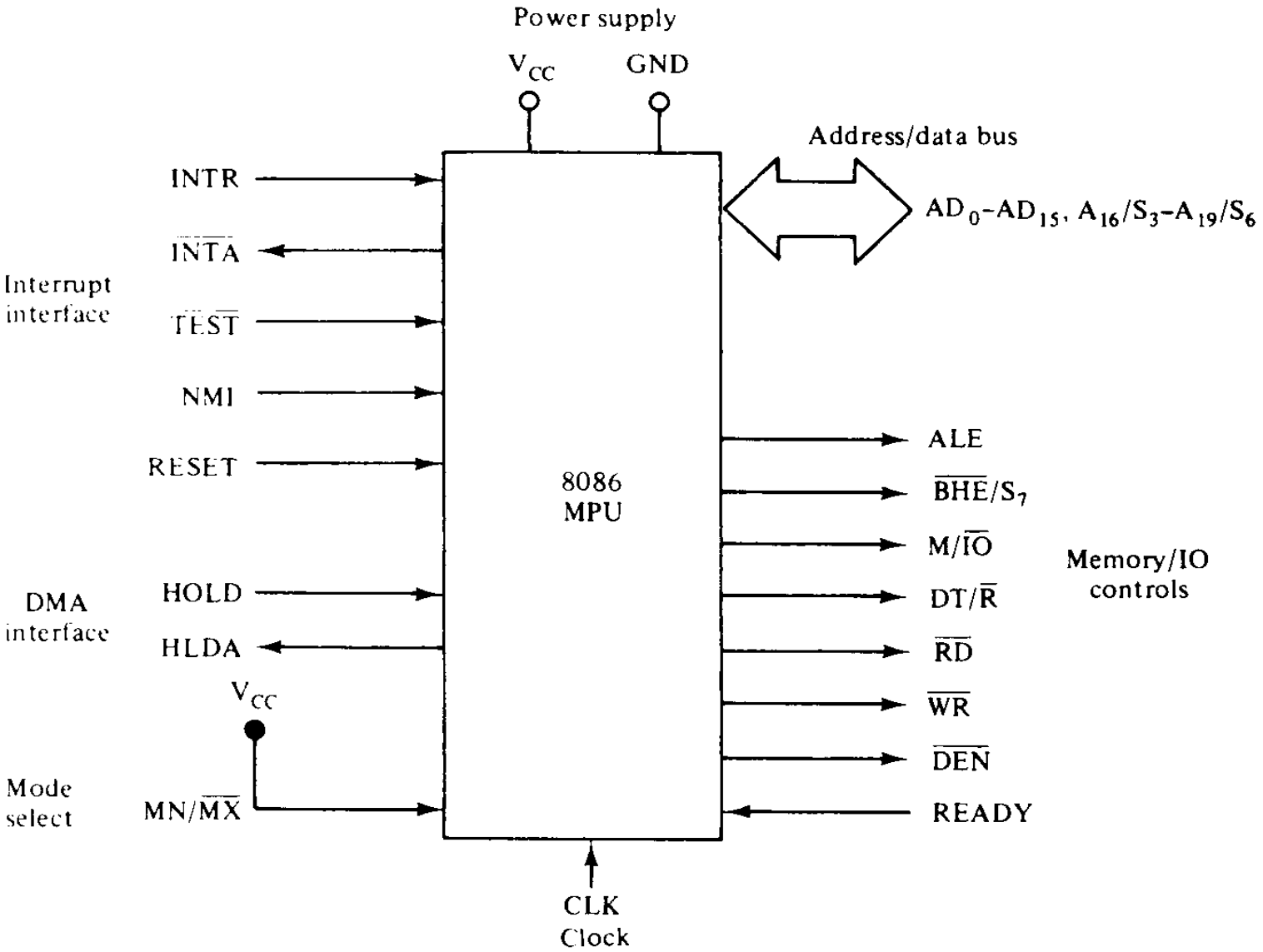
Minimum mode unique signals

Minimum mode signals ($MN/\overline{MX} = V_{CC}$)		
Name	Function	Type
HOLD	Hold request	Input
HLDA	Hold acknowledge	Output
$\overline{WR}$	Write control	Output, 3-state
IO/$\overline{M}$	IO/memory control	Output, 3-state
DT/$\overline{R}$	Data transmit/receive	Output, 3-state
$\overline{DEN}$	Data enable	Output, 3-state
$\overline{SSO}$	Status line	Output, 3-state
ALE	Address latch enable	Output
$\overline{INTA}$	Interrupt acknowledge	Output

8088 Minimum-mode block diagram



8086 Minimum-mode block diagram



9.1: 8088 MICROPROCESSOR data bus

– Due to chip packaging limitations in the 1970s, there was great effort to use the minimum number of pins
for external connections.
  - Intel multiplexed address & data buses, using the same pins to carry two sets of information: address & data.

– Pins 9-16 (**AD0–AD7**) are used for both data and addresses in 8088.
  - **AD** stands for "address/data."
– The **ALE** (address latch enable) pin signals whether the information on pins AD0–AD7 is address or data.

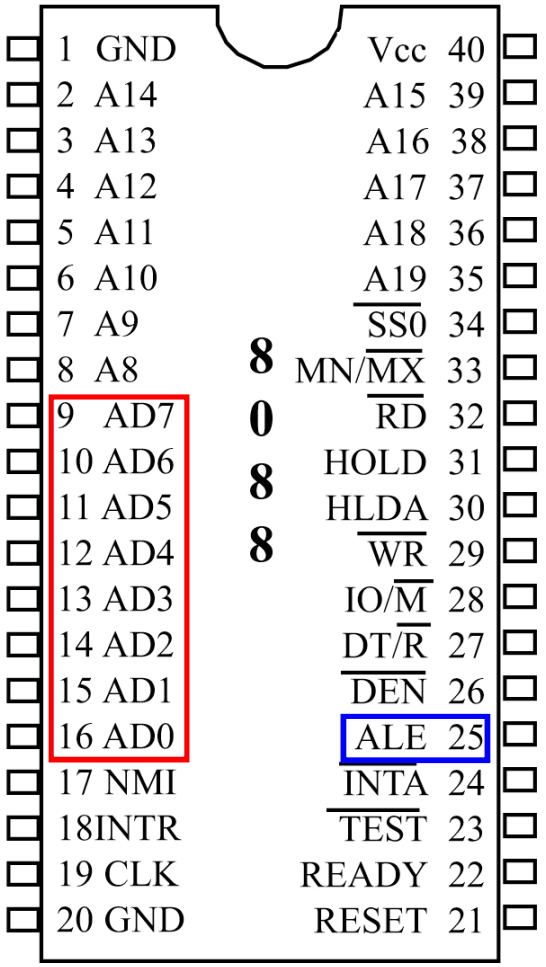


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR data bus

– When 8088 sends out an address, it activates (sets *high*) the **ALE**, to indicate the information on pins **AD0**–**AD7** is the *address* (**A0**–**A7**).
  - This information must be *latched*, then pins AD0–AD7 are used to carry data.

– When data is to be sent out or in, **ALE** is low, which indicates that **AD0**–**AD7** will be used as *data* buses (**D0**–**D7**).

– The process of separating address and data from pins AD0–AD7 is called *demultiplexing*.

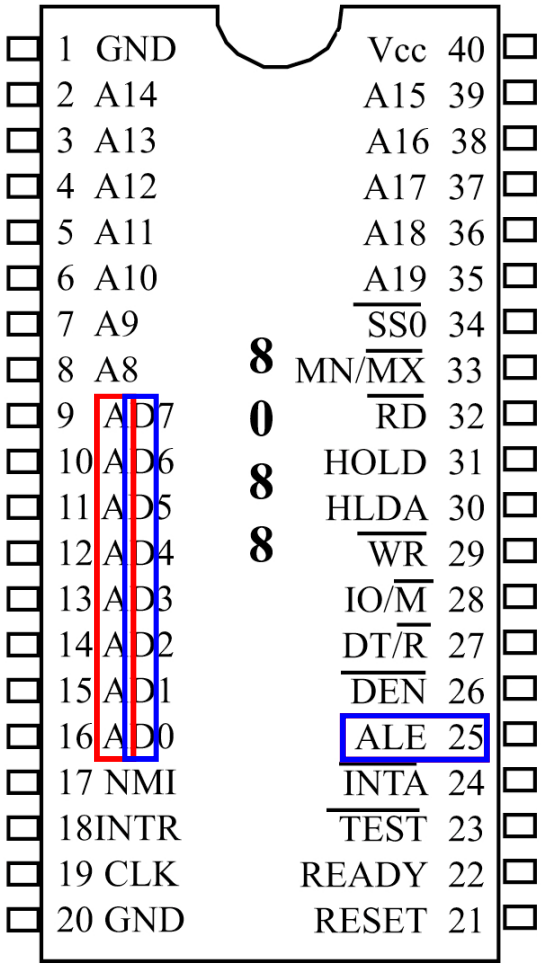


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR address bus

- 8088 has 20 address pins (**A0**–**A19**), allowing it to address a maximum of one megabyte of memory (2^{20} = 1M).
  - To demultiplex address signals, a latch must be used to grab the addresses.

- Widely used is the 74LS373 IC, also 74LS573, a 74LS373 variation.
  - **AD0** to **AD7** go to the 74LS373 latch, providing the 8-bit address **A0**–**A7**.
  - **A8**–**A15** come directly from the microprocessor (pins **2**–**8** & pin **39**).
- The last 4 bits of the address come from **A16**–**A19**, pin numbers **35**–**38**.

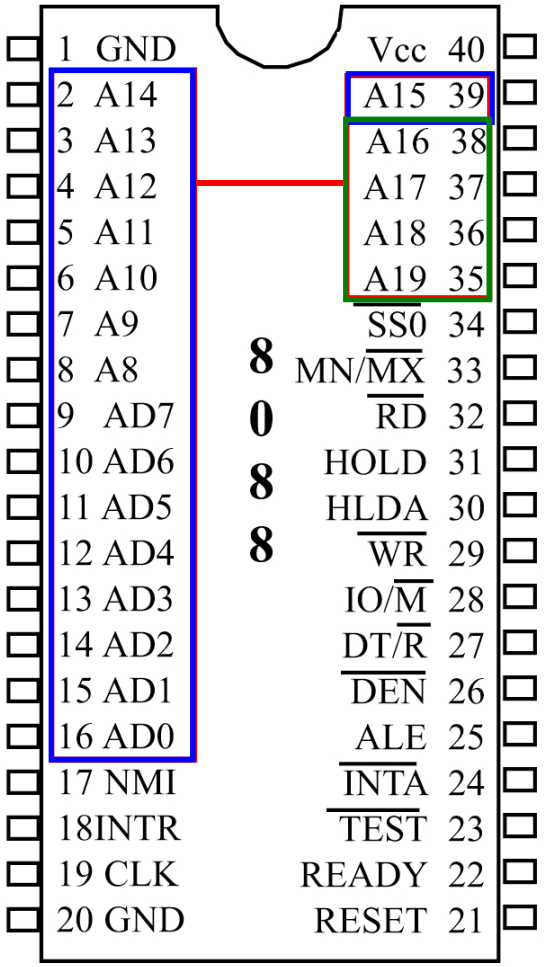


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR address bus

The most widely used latch is the 74LS373 IC.
Also used is the 74LS573, a 74LS373 variation.

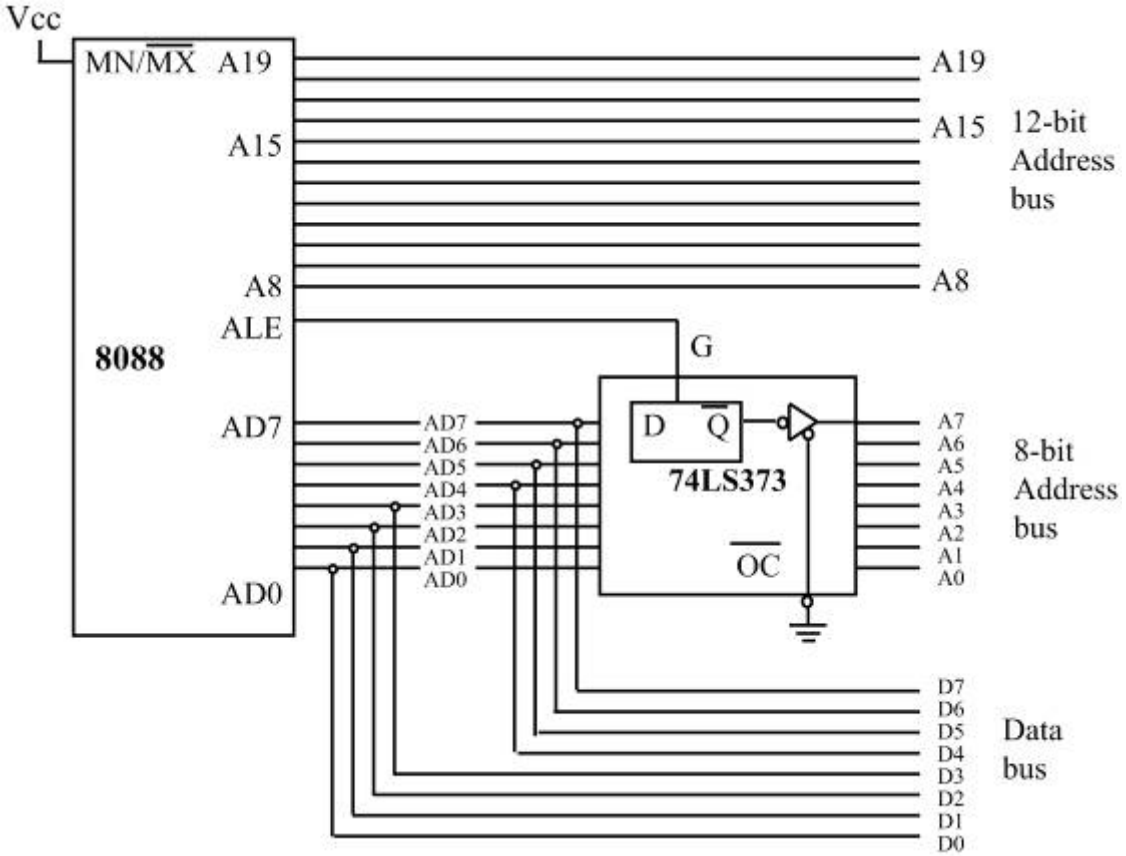
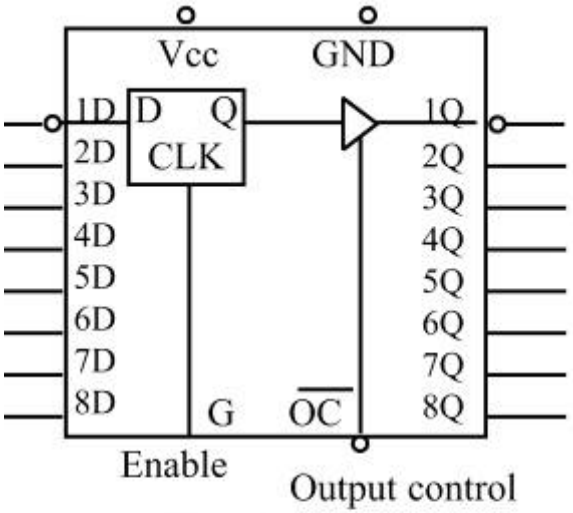


Fig. 9-2 Role of ALE in address/data demultiplexing



Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Fig. 9-3 74 LS373 D Latch

9.1: 8088 MICROPROCESSOR address bus

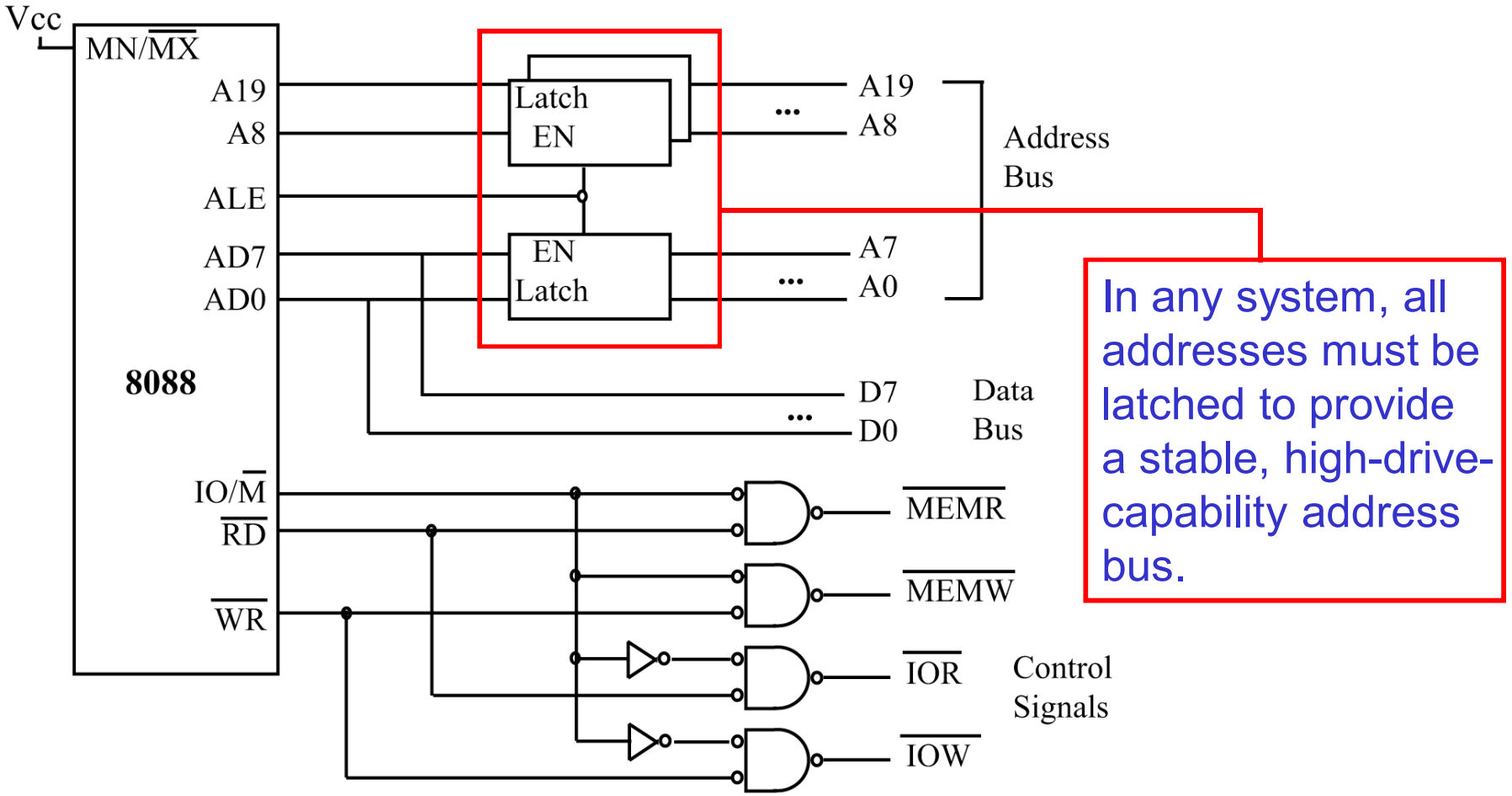


Fig. 9-5 Address,Data,and Control Buses in 8088-based System

9.1: 8088 MICROPROCESSOR control bus

- 8088 can access both memory and I/O devices for read and write operations, four operations, which need four control signals:
  - **MEMR** (memory read); **MEMW** (memory write).
  - **IOR** (I/O read); **IOW** (I/O write).

9.1: 8088 MICROPROCESSOR control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
    - RD & WR pins are both *active-low*.
    - IO/M is *low* for memory, *high* for I/O devices.

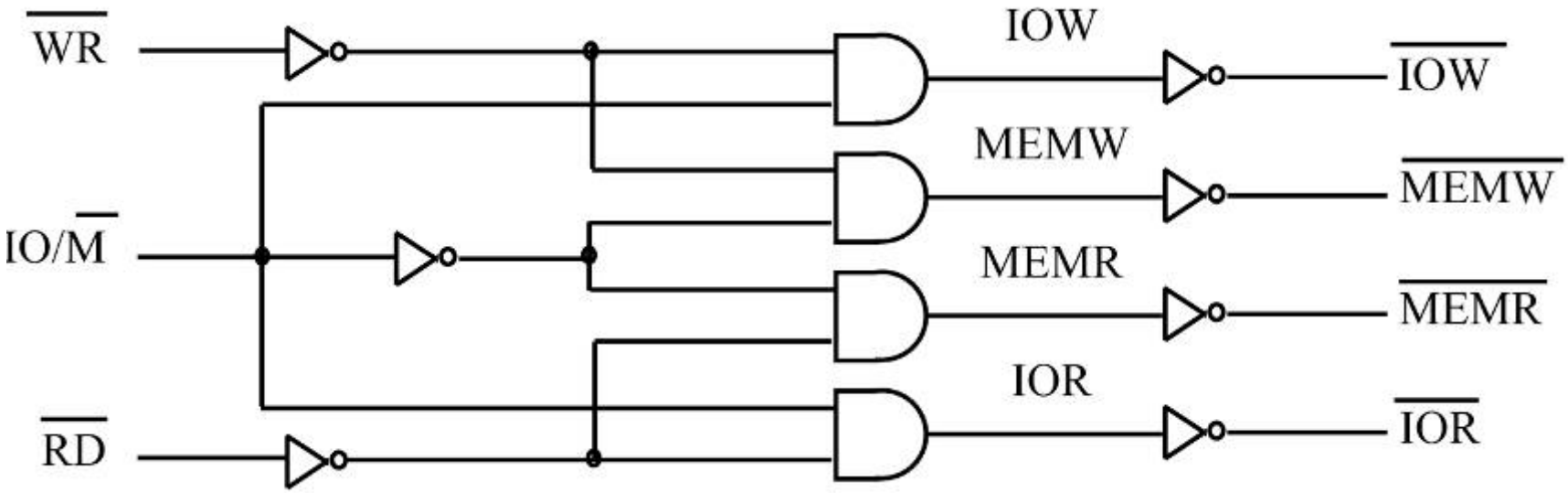


Fig. 9-4 Control signal generation

9.1: 8088 MICROPROCESSOR control bus

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
    - $\overline{RD}$ & $\overline{WR}$ pins are both *active-low*.
    - IO/$\overline{M}$ is *low* for memory, *high* for I/O devices.

Four control signals are generated:

$\overline{IOR}$; **$\overline{IOW}$**; **$\overline{MEMR}$**; **$\overline{MEMW}$**.

All of these signals must be active-low.

Table 9-1: Control Signal Generation

RD	WR	IO/M	Signal
0	1	0	$\overline{MEMR}$
1	0	0	$\overline{MEMW}$
0	1	1	$\overline{IOR}$
1	0	1	$\overline{IOW}$
0	0	x	Never happens

9.1: 8088 MICROPROCESSOR control bus

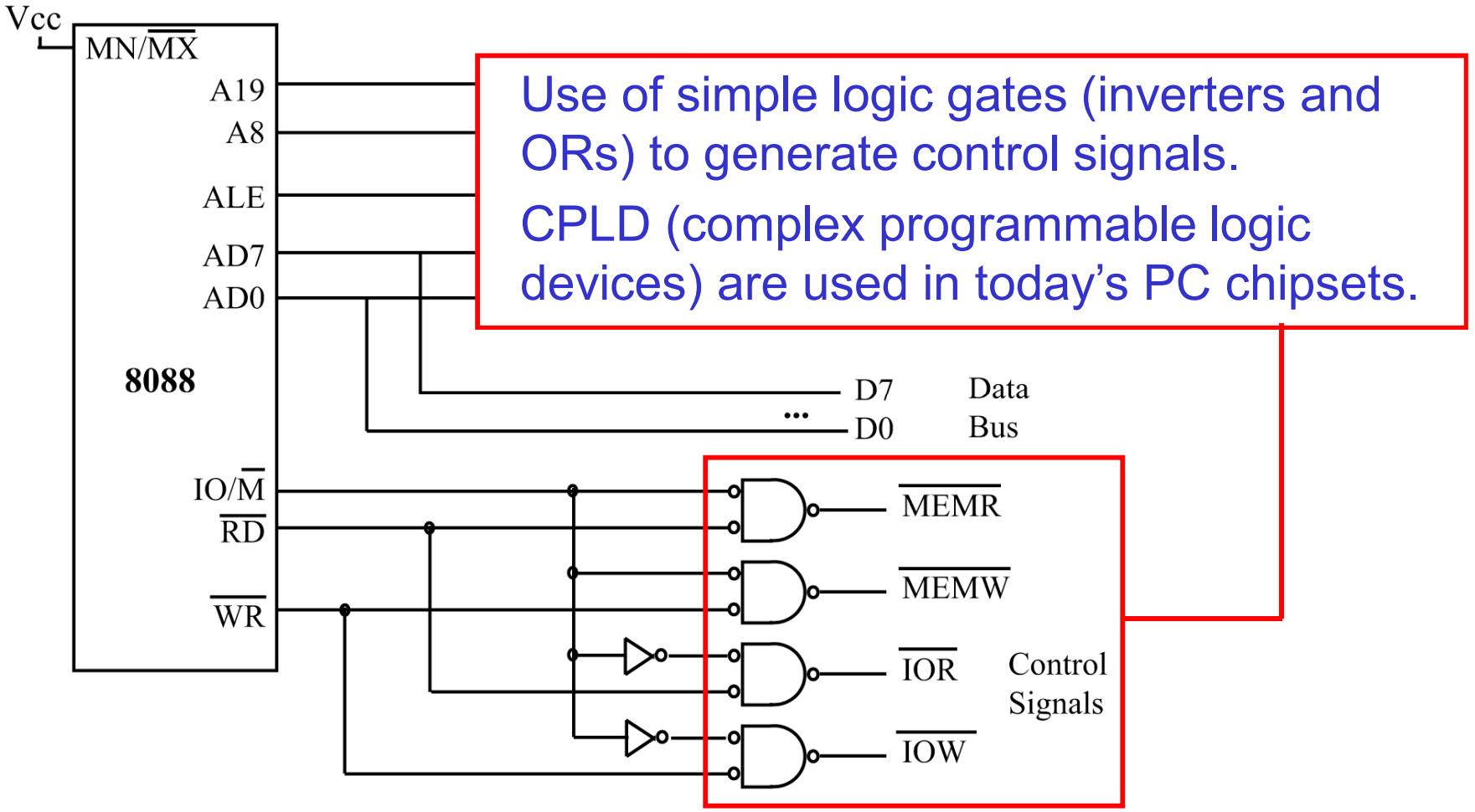


Fig. 9-5 Address,Data,and Control Buses in 8088-based System

Minimum Mode Interface

- Address/Data bus: 20 bits/8 bits (AD0-AD7) multiplexed for 8088
- Address/Data bus: 20 bits/16 bits (AD0-AD15) multiplexed for 8086
- Status signals: A_{16}-A_{19} multiplexed with status signals S_3-S_6 respectively
  - **S3 and S4 together** form a 2 bit binary code that identifies which of the internal segment registers were used to generate the physical address that was output on the address bus during the current bus cycle.
  - **S5** is the logic level of the **IF**,
  - **S6 is always logic 0**. S0,S1,S2 used in maxmode (later)

S4	S3	Address status
0	0	Alternate(relative to ES segment)
0	1	Stack (relative to SS Segment)
1	0	Code/None (relative to CS segment or a default zero)
1	1	Data (relative to DS segment)

Minimum Mode Interface

- Control Signals: (8088)
  - ✓ **Address Latch Enable (ALE)** is a pulse to logic 1 that signals external circuitry when a valid address is on the bus. This address can be latched in external circuitry on the 1-to-0 edge of the pulse at ALE.
  - ✓ **IO/$\overline{M}$ line:** memory or I/O transfer is selected (complement for 8086)
  - ✓ **DT/R line**: direction of data is selected
  - ✓ **$\overline{RD}$ line: =**0 when a read cycle is in progress
  - ✓ **$\overline{WR}$ line:** =0 when a write cyle is in progress
  - ✓ **$\overline{DEN}$ line: (Data enable)** Enables the external devices to supply data to the processor. Used when sharing memory with another processor.

9.1: 8088 MICROPROCESSOR
address bus

The most widely used latch is the 74LS373 IC.
Also used is the 74LS573, a 74LS373 variation.

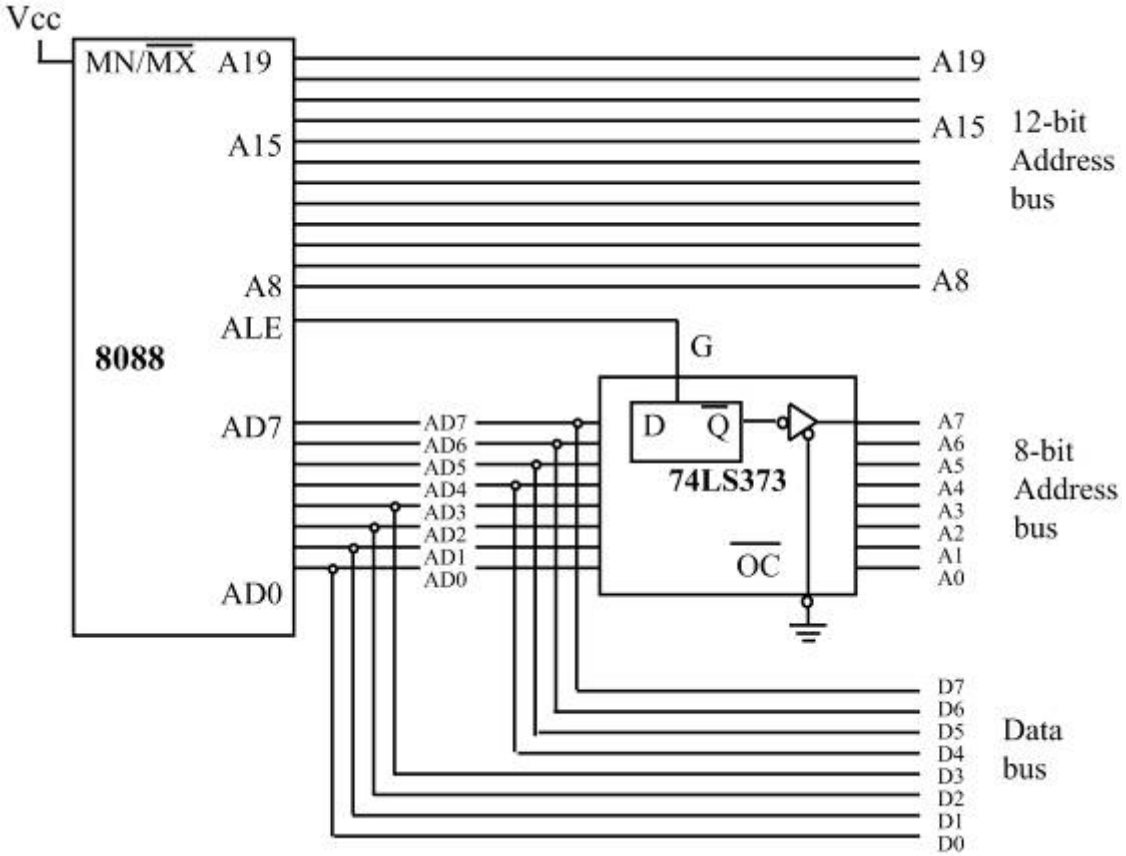
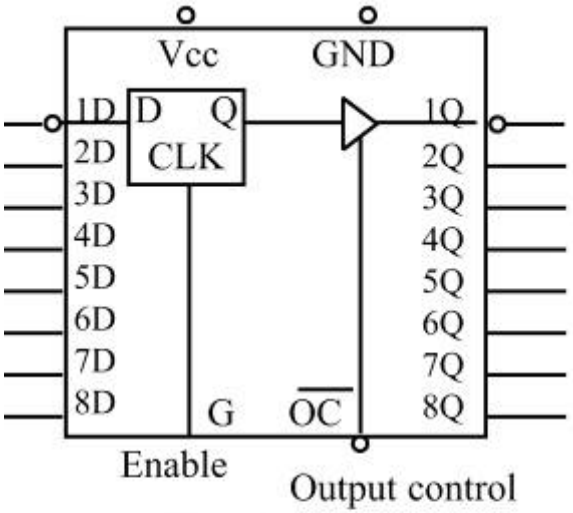


Fig. 9-2 Role of ALE in address/data demultiplexing



Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Fig. 9-3 74 LS373 D Latch

Control Signals: (8088)

SSO (System Status Output) line (only for 8088)

=1 when data is read from memory and =0 when code is read from memory

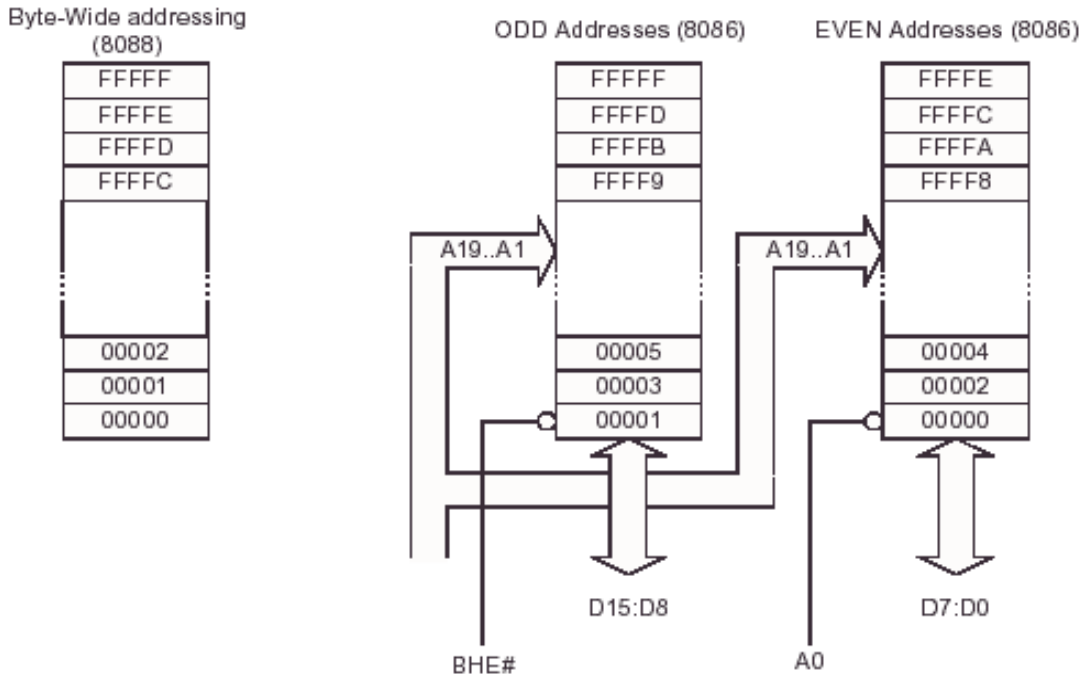
IO/M	DT/R	SS0	FUNCTION
0	0	0	Interrupt Acknowledge
0	0	1	Memory Read
0	1	0	Memory Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	I/O Read
1	1	0	I/O Write
1	1	1	Passive

Minimum Mode Interface

✓**BHE (Bank High Enable) line** (8086 only) :=0 for most significant byte of data and also carries S_7=1

BHE#	A0	Selection
0	0	Whole word (16-bits)
0	1	High byte to/from odd address
1	0	Low byte to/from even address
1	1	No selection

This is how memory is accessed using these signals:



Data Transfer

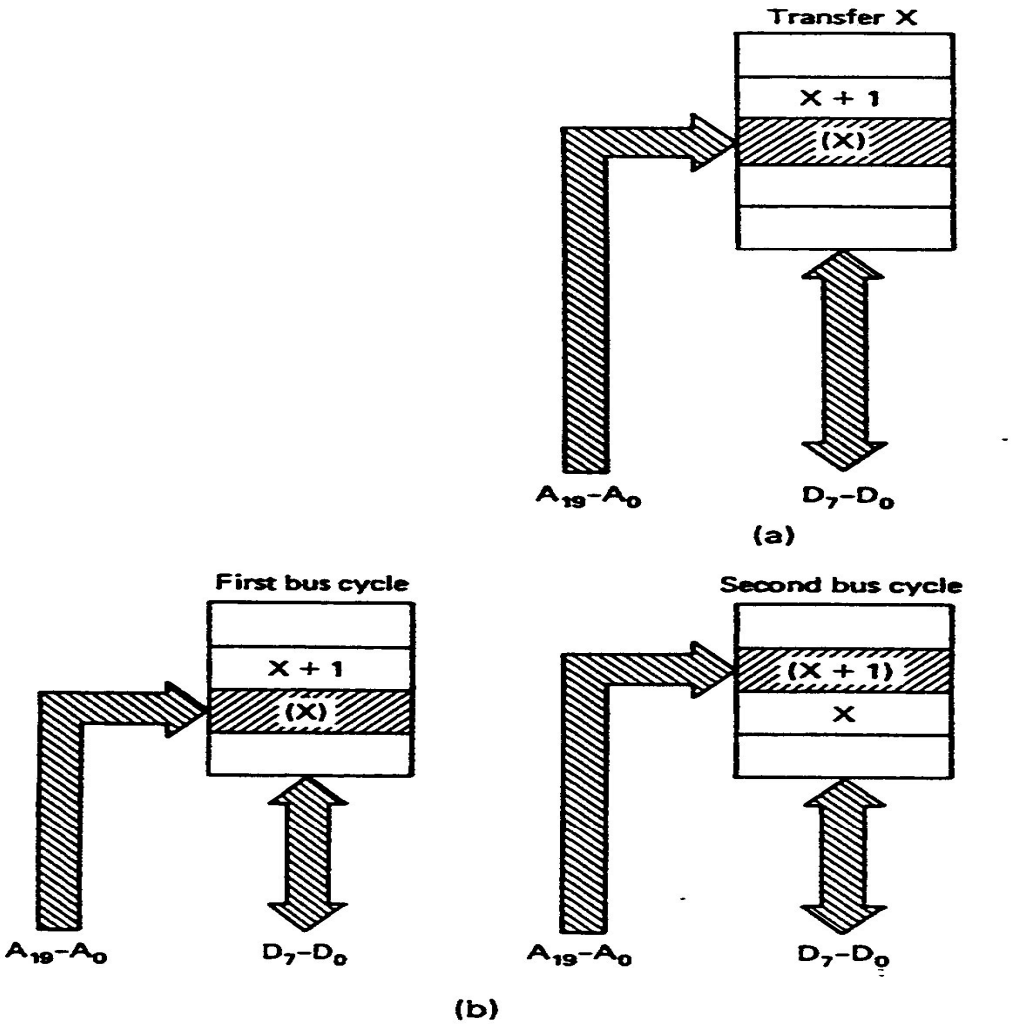
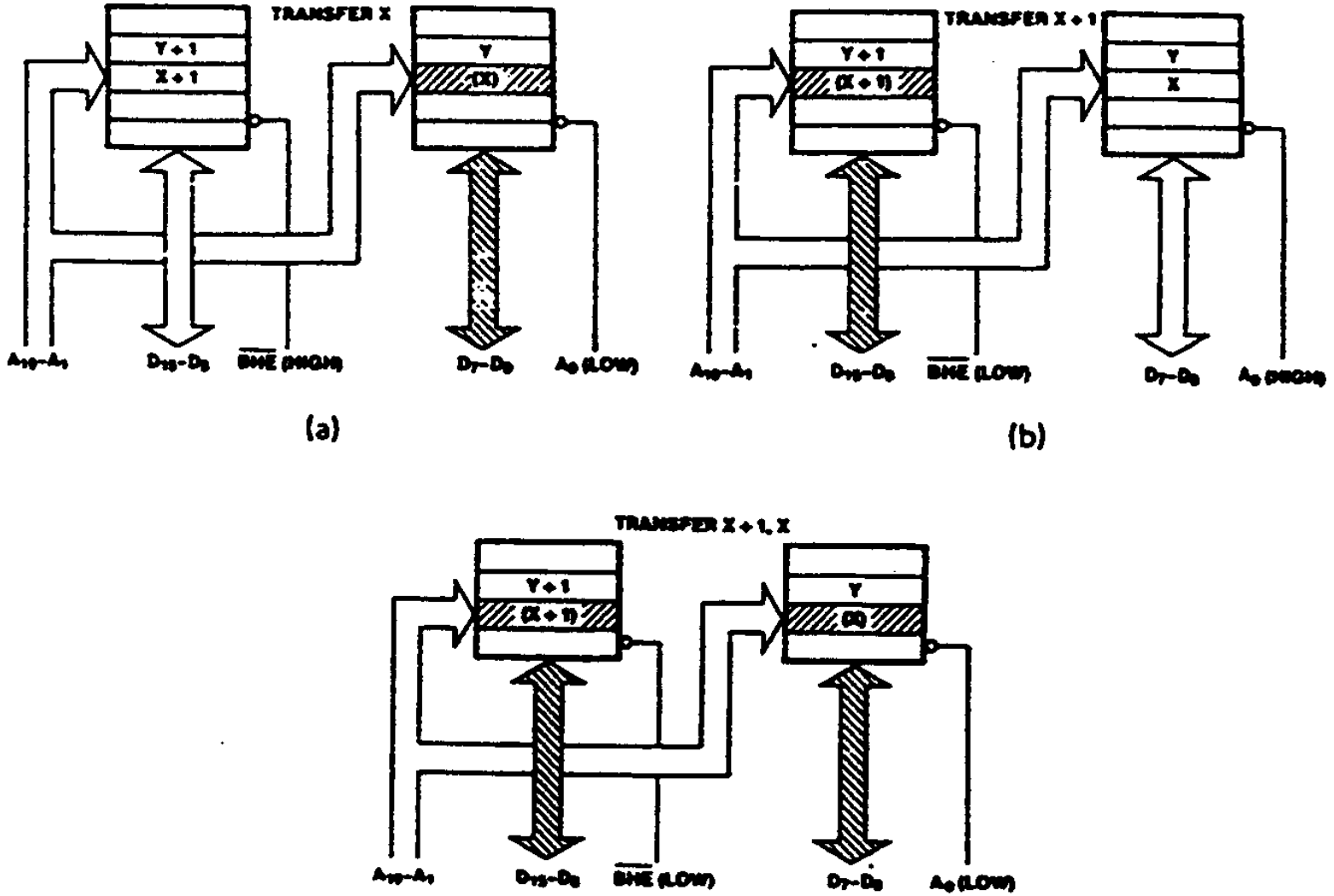
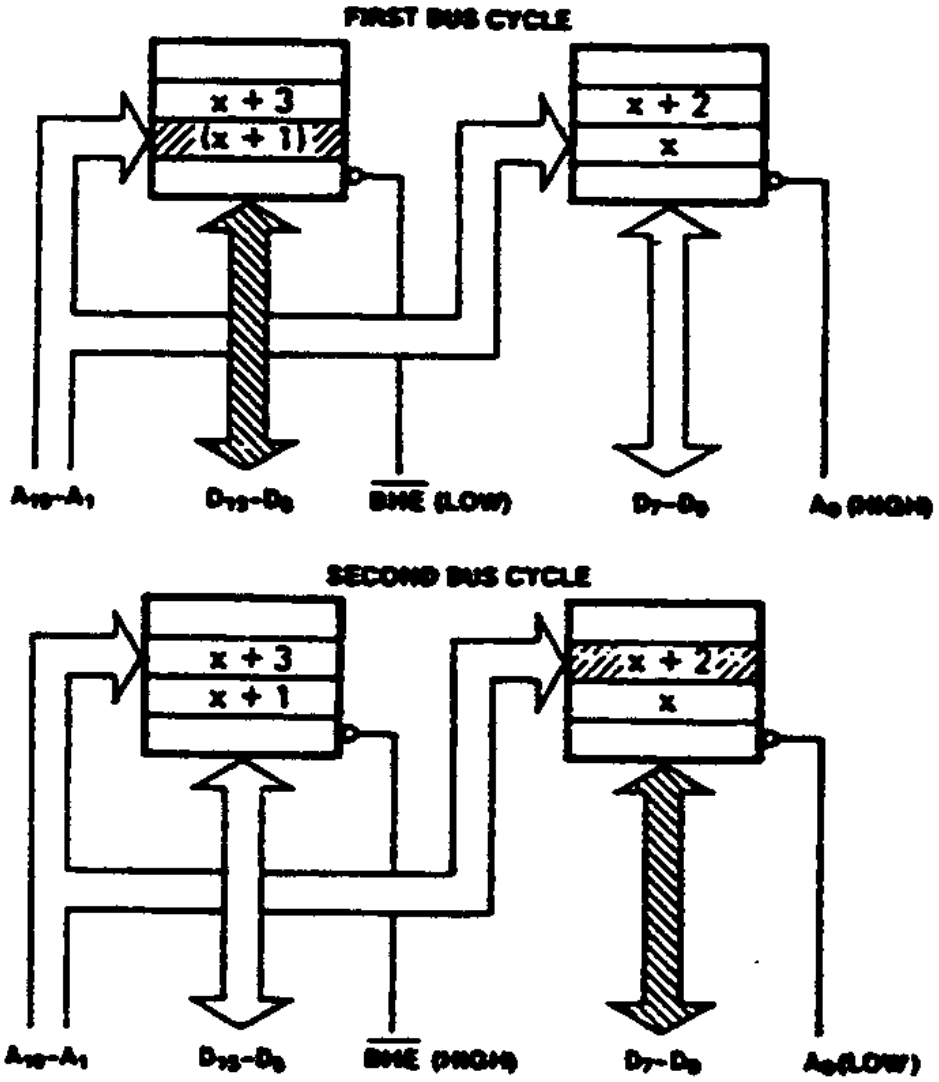


Figure 8–16 (a) Byte tnasfer by the 8088. (b) Word transfer by the 8088.

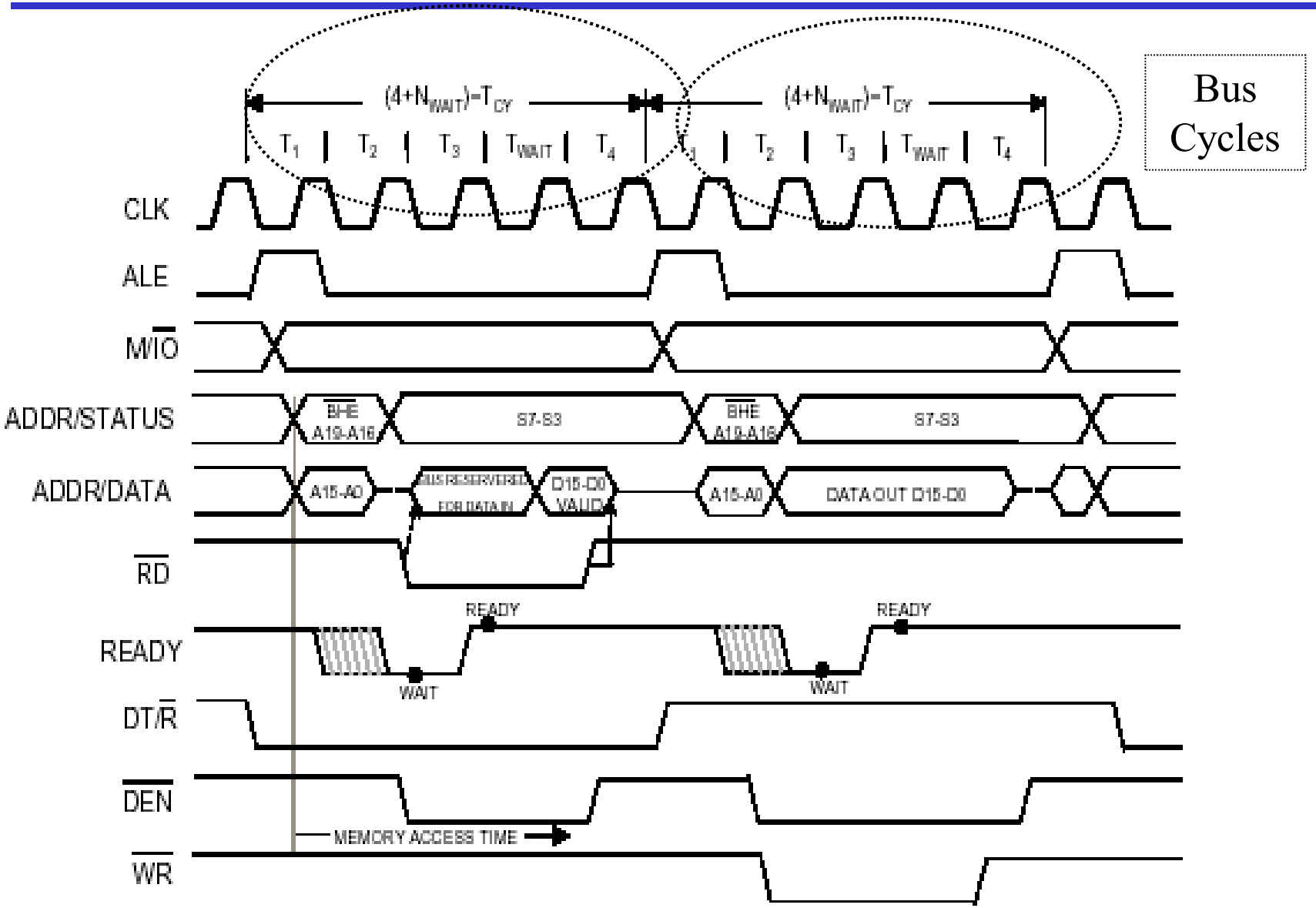

TRANSFER X
Y + 1
X + 1
Y
(X)
A_{19}–A_1
D_{15}–D_8
$\overline{BHE}$ (HIGH)
D_7–D_0
A_0 (LOW)
(a)
TRANSFER X + 1
Y + 1
(X + 1)
Y
X
A_{19}–A_1
D_{15}–D_8
$\overline{BHE}$ (LOW)
D_7–D_0
A_0 (HIGH)
(b)
TRANSFER X + 1, X
Y + 1
(X + 1)
Y
(X)
A_{19}–A_1
D_{15}–D_8
$\overline{BHE}$ (LOW)
D_7–D_0
A_0 (LOW)
(c)


FIRST BUS CYCLE
x + 3
(x + 1)
x + 2
x
SECOND BUS CYCLE
x + 3
x + 1
x + 2
x

Bus Cycle and Time States

- A bus cycle (machine cycle) defines the basic operation that a microprocessor performs to communicate with external devices
- Examples of bus cycles are memory read, memory write, input/output read and input/output write.
- A bus cycle corresponds to a sequence of events that starts with an address being output on the system bus followed by a read or write data transfer
- During these operations, a series of control signals are also produced by the MPU to control the direction and timing of the bus.
- Each bus cycle consists of at least four clock periods: T1, T2, T3, and T4.
- These clock periods are also called the T-States

Bus Cycle and Time States



9.1: 8088 MICROPROCESSOR
bus timing of the 8088

– 8088 uses 4 clocks for memory & I/O bus activities.
  - In read timing, **ALE** latches the address in the first clock cycle.
  - In the second and third cycles, the read signal is provided.
  - By the end of the fourth, data must be at the CPU pins.
  - The entire read or write cycle time is only 4 clock cycles.

If reading/writing takes more than 4 clocks, wait states (WS) can be requested from the CPU.

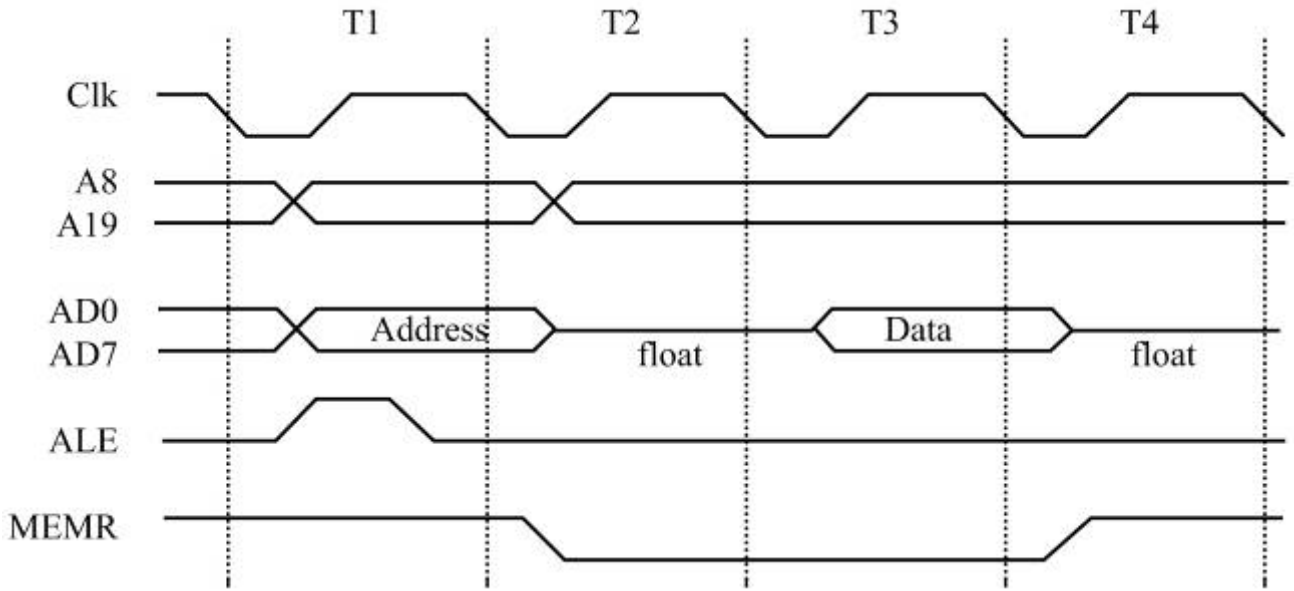


Fig. 9-6 ALE Timing

Bus Cycle and Time States

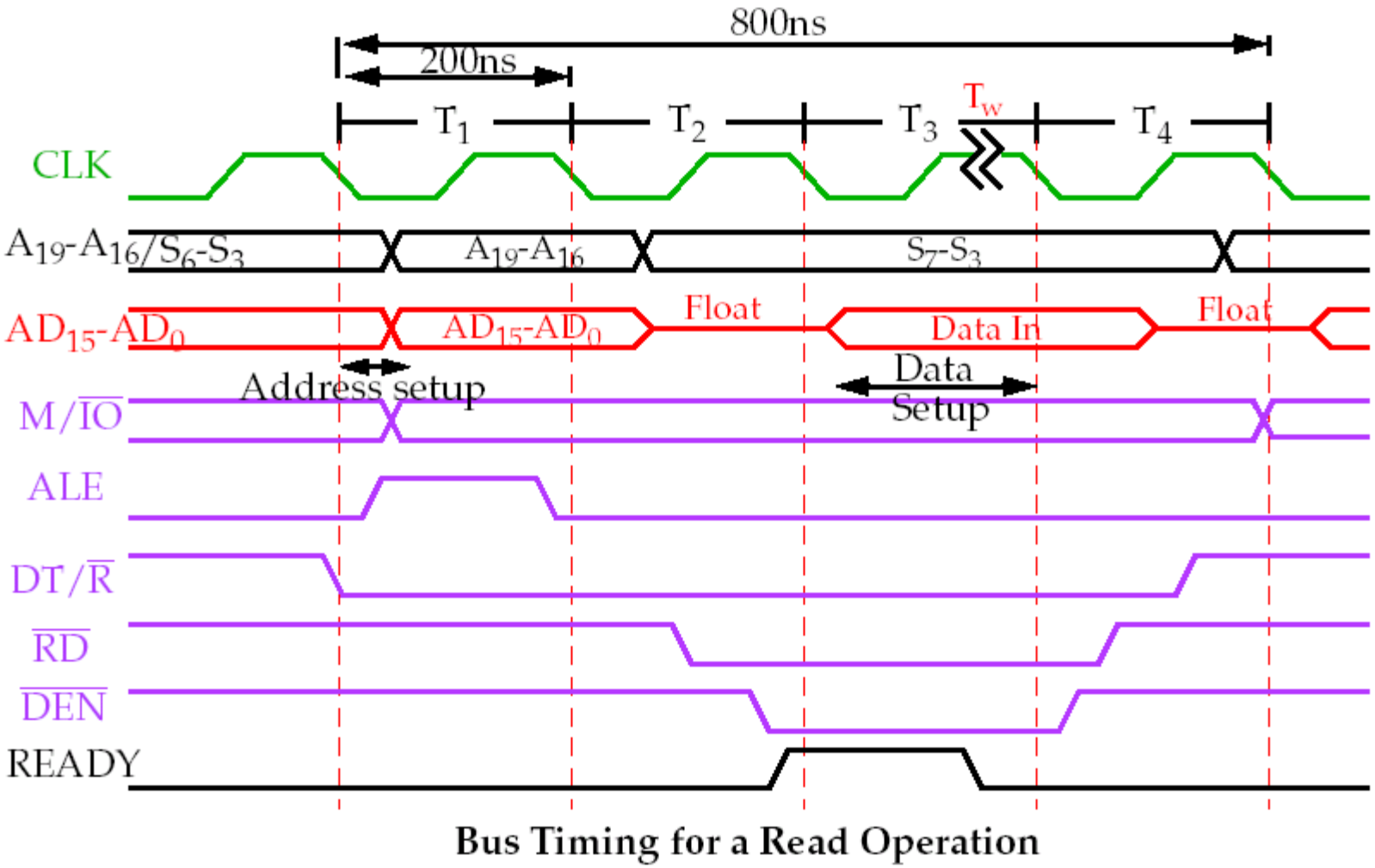
T1 - start of bus cycle. Actions include setting control signals (or S0-S2 status lines) to give the required values for ALE, DTR IO/M putting a valid address onto the address bus.

T2 - **the RD or WR control signals are issued, DEN is asserted and in the case of a write, data is put onto the data bus. The DEN turns on the data bus buffers to connect the CPU to the external data bus. The READY input to the CPU is sampled at the end of T2 and if READY is low, a wait state T_W (one or more) is inserted before T3 begins.**

T3 - this clock period is provided to allow memory to access the data. If the bus cycle is a read cycle, the data bus is sampled at the end of T3.

T4 - **all bus signals are deactivated in preparation for the next clock cycle. The 8088 also finishes sampling the data (in a read cycle) in this period. For the write cycle, the trailing edge of the WR signal transfers data to the memory or I/O, which activates and write when WR returns to logic 1 level.**

Read Cycle of the 8086

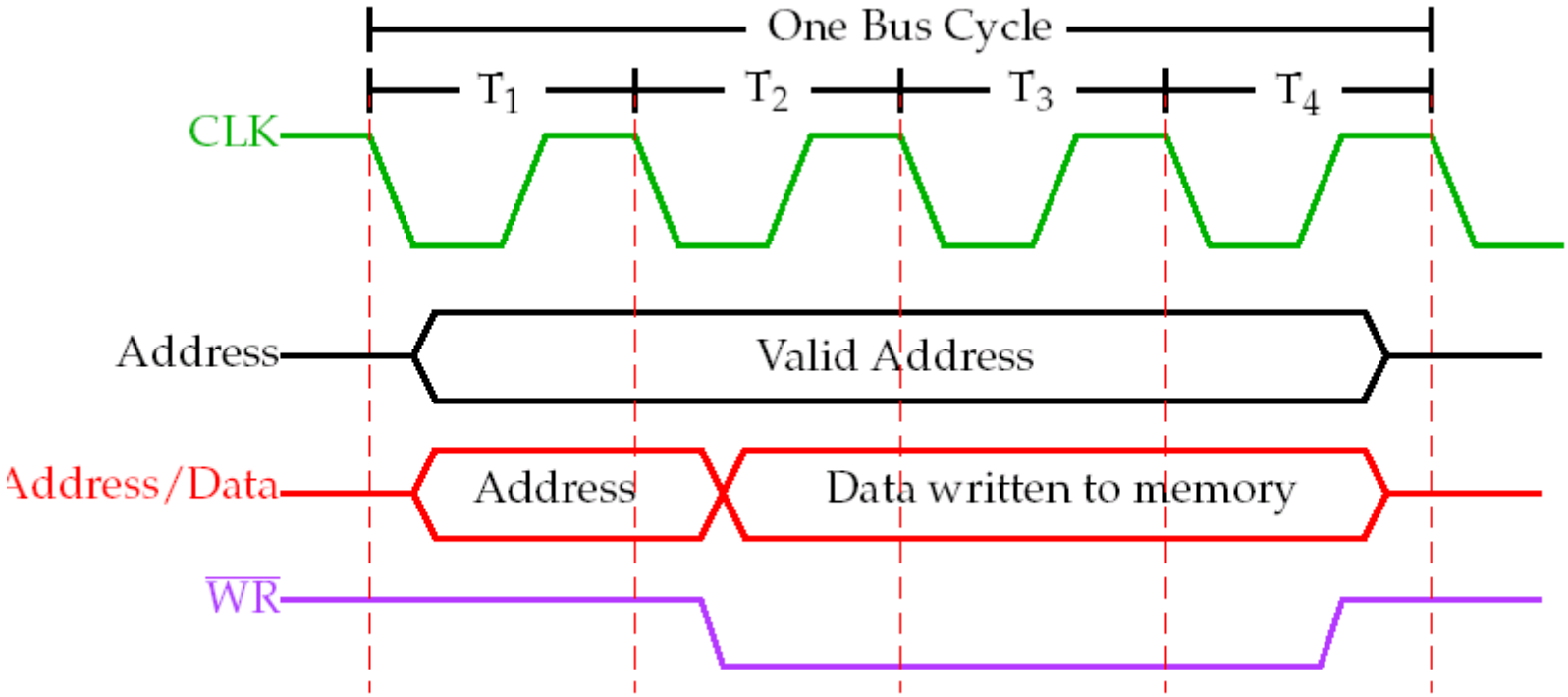


Bus Timing for a Read Operation

Read Cycle

- Each BUS CYCLE (machine cycle) on the 8086 equals **four** system clocking periods (T states).
- The clock rate is **5MHz**, therefore one Bus Cycle is *800ns*.
- Memory specs (memory access time) must match constraints of system timing.
- For example, bus timing for a read operation shows almost *600ns* are needed to read data.
- However, memory must access faster due to setup times, e.g.
- Address setup and data setup.
- This subtracts off about *150ns*.
- Therefore, memory must access in at least *450ns* minus another *30-40ns* guard band for buffers and decoders.
- *420ns* DRAM required for the 8086.

Write Cycle in 8088/8086 Minmode



Simplified 8086 Write Bus Cycle

9.1: 8088 MICROPROCESSOR other pins

– Pins 24–32 have different functions depending on whether 8088 is in minimum or maximum mode.
  - In maximum mode, 8088 needs supporting chips to generate the control signals.

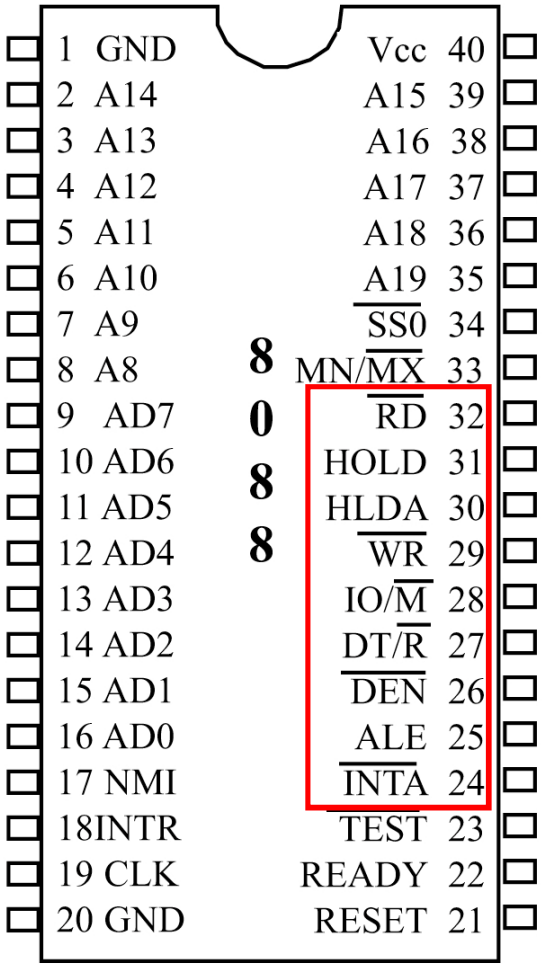


Fig. 9-1a 8088 in minimum mode

9.1: 8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
24	INTA (interrupt acknowledge) Active-low output signal. Informs interrupt controller that an INTR has occurred and that the vector number is available on the lower 8 lines of the data bus.
25	ALE (address latch enable) Active-high output signal. Indicates that a valid address is available on the external address bus.
26	DEN (data enable) Active-low output signal. Enables the 74LS245. This allows isolation of the CPU from the system bus.
27	DT/R (data transmit/receive) Active-low output signal used to control the direction of data flow through the 74LS245 transceiver.
28	IO/M (input-output or memory) Indicates whether the address bus is accessing memory or an I/O device. In the 8088, it is low when accessing memory and high when accessing I/O. This pin is used along with RD and WR pins to generate the four control signals MEMR, MEMW, IOR, and IOW.

9.1: 8088 MICROPROCESSOR other pins

Functions of 8088 pins 24–32 in minimum mode.

Table 9-2: Pins 24–32 in Minimum Mode

Pin	Name and Function
29	WR (write) Active-low output signal. Indicates that the data on the data bus is being written to memory or an I/O device. Used along with signal IO/M (pin 28) to generate the MEMW and IOW control signals for write operations.
30	HLDA (hold acknowledge) Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that the DMA controller can use the buses.
31	HOLD (hold) Active-high input from the DMA controller that indicates that the device is requesting access to memory and I/O space and that the CPU should release control of the local buses.
32	RD (Read) Active-low output signal. Indicates that the data is being read (brought in) from memory or I/O to the CPU. Used along with signal IO/M (pin 28) to generate MEMR and IOR control signals for read operations.

Minimum Mode Interface

- DMA (Direct Memory Access) Interface Signals:
  - HOLD: External device puts logic level 1 to HOLD input to take control of the bus for DMA request. (sampled at every rising edge of the CLK)
  - $\overline{\text{HLDA}}$ (Hold acknowledge) : Processor responds by putting logic level 1 to HLDA. (at the end of T4)
  - In this state; Address and Data lines, SSO, IO/$\overline{\text{M}}$, DT/$\overline{\text{R}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DEN}}$ signals are all put to high-Z state

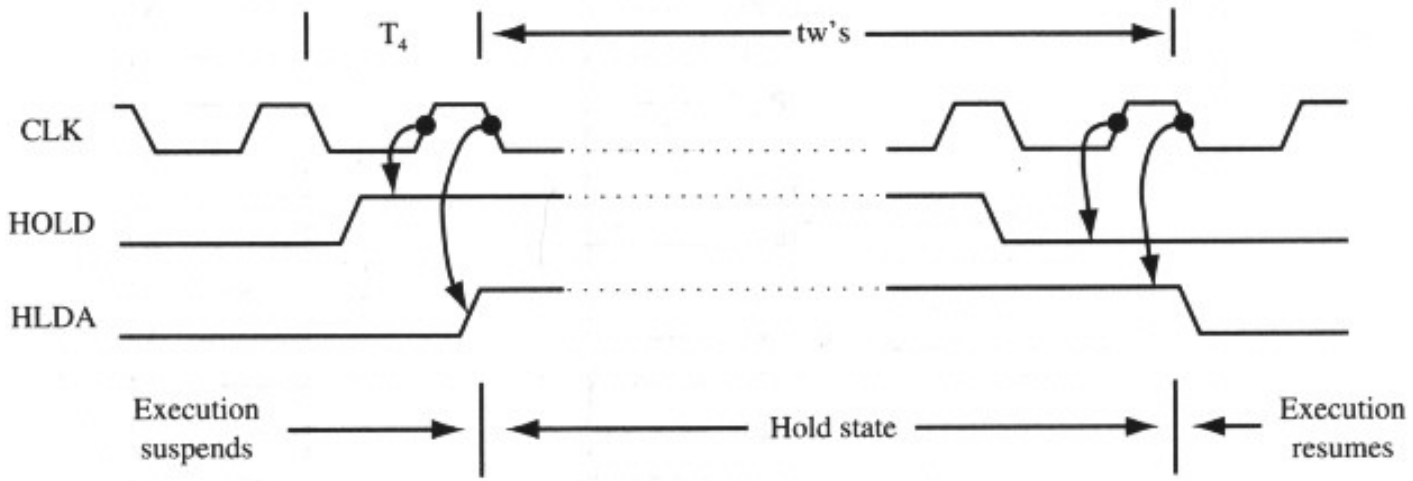


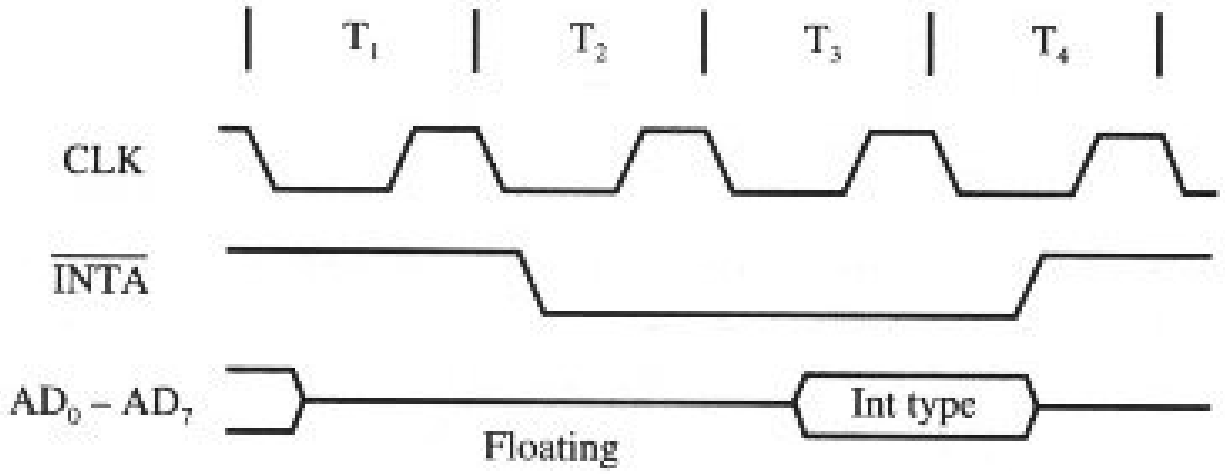
FIGURE 10.14 HOLD timing

9.1: 8088 MICROPROCESSOR other pins

- **MN/MX** (minimum/maximum) - minimum mode is selected by connecting MN/MX (pin number 33) directly to +5 V.
  - Maximum mode is selected by grounding this pin.
- **CLOCK** - an input signal, connected to the 8284 clock generator.

Minimum Mode Interface

- Interrupt signals:
  - **INTR (Interrupt request)** :=1 shows there is a service request, sampled at the final clock cycle of each instruction acquisition cycle.
  - **INTA** : @T1 tri-states the Address Bus. Processor responds with two pulses going to 0 when it services the interrupt and waits for the interrupt service number after the second pulse.



(a) Minmode

9.1: 8088 MICROPROCESSOR other pins

- **TEST** - in maximum mode, an input from the 8087 math coprocessor to coordinate communications. Processor suspends operation when=1. Resumes operation when=0. Used to syncronize the processor to external events. (All 8087-capable compilers and assemblers automatically generate a **WAIT** instruction before each coprocessor instruction. The **WAIT** instruction tests the CPU's **TEST** pin and suspends execution until its input becomes "**LOW**". When **TEST=0, WAIT** instruction is like **NOP**.
  - In all 8086/8087 systems, the 8086 /TEST pin is connected to the 8087 BUSY pin. As long as the EU executes a coprocessor instruction, it forces its BUSY pin "HIGH"; thus, the WAIT opcode preceding the coprocessor instruction stops the CPU until any still-executing coprocessor instruction has finished)
  - Not used In minimum mode.!

9.1: 8088 MICROPROCESSOR other pins

- **RESET** - terminates present activities of the processor when a *high* is applied to the **RESET** input pin.
- **RESET** : =0. Need at least 4 clock cycles. Issuing reset causes the processor to fetch the first instruction from the memory FFFF:0000h.

A presence of *high* will force the microprocessor to stop all activity and set the major registers to the values shown at right.

Table 9-3: IP and Segment Register Contents after Reset

Register	Contents
CS	FFFF
IP	0000
DS	0000
SS	0000
ES	0000

Interrupt Signals cont'd

Interrupt	Logic	Disabled by SW?	Priority
NMI	Rising Edge	No	High
INTR	High	Yes	Low

–**NMI (Nonmaskable interrupt) :** A leading edge transition causes the processor go to the interrupt routine after the current instruction is executed.

–**NMI** (nonmaskable interrupt) - an edge-triggered (*low* to *high*) input signal to the processor that will make the microprocessor jump to the interrupt vector table after it finishes the current instruction.

–Cannot be masked by software.

Minimum Mode Interface

•READY Control line:

–can be used to insert wait states into the bus cycle so that it is extended by a number of clock periods.

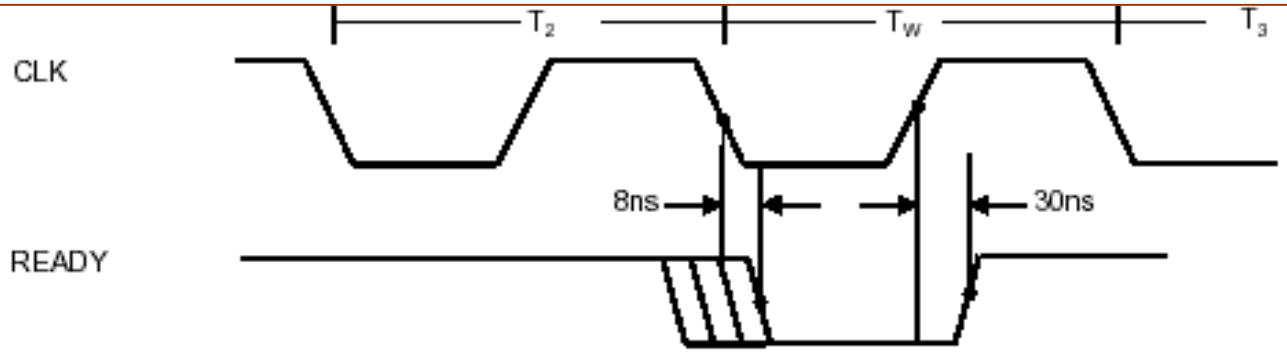
READY - an input signal, used to insert a wait state for slower memories and I/O. It inserts wait states when it is *low*.

✓If the access time for a memory device is longer than the memory access time calculated, need to give extra clock periods, wait state Tw, for memory.

✓The READY input is sampled at the end of T2 and again, if applicable, in the middle of Tw. If READY is a logic 0 on 1-to-0 clock transition, then Tw is inserted between T2 and T3. And will check for logic 1 on 0-to-1 clock transition in the middle of Tw to see if it shall go back T3.

✓During the wait state, signals on the buses remain the same as they were at the start of the WAIT state.

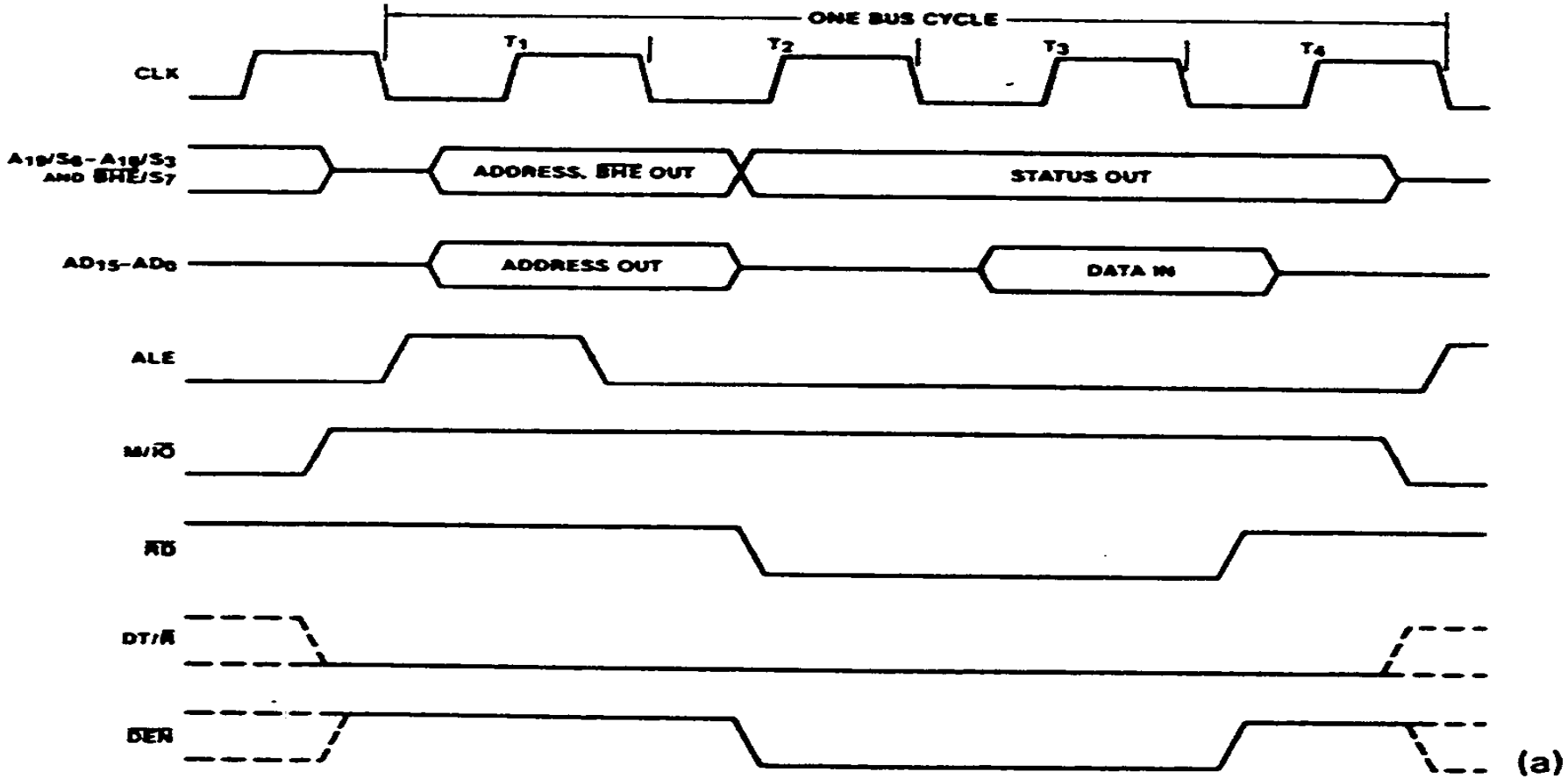
✓By having the WAIT state, slow memory and devices has at least one more cycle (200ns for 5 MHz 8088) to get its data output.



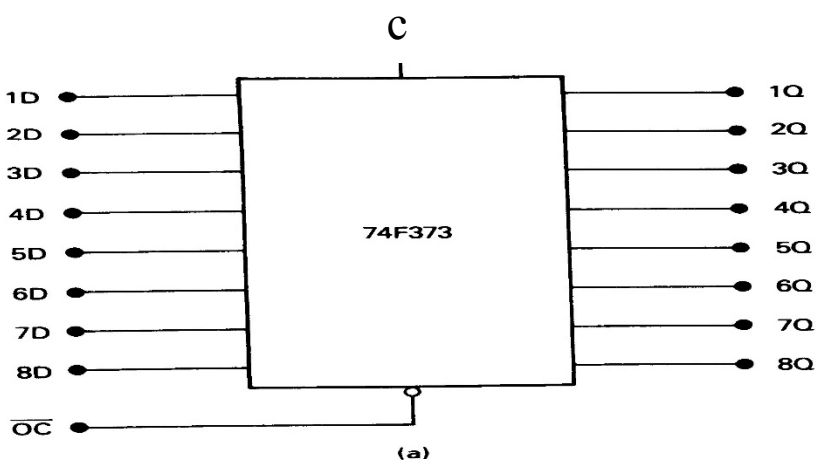
(a) 8088/86 READY Input Timing

Read Cycle of the 8086 - minimum mode

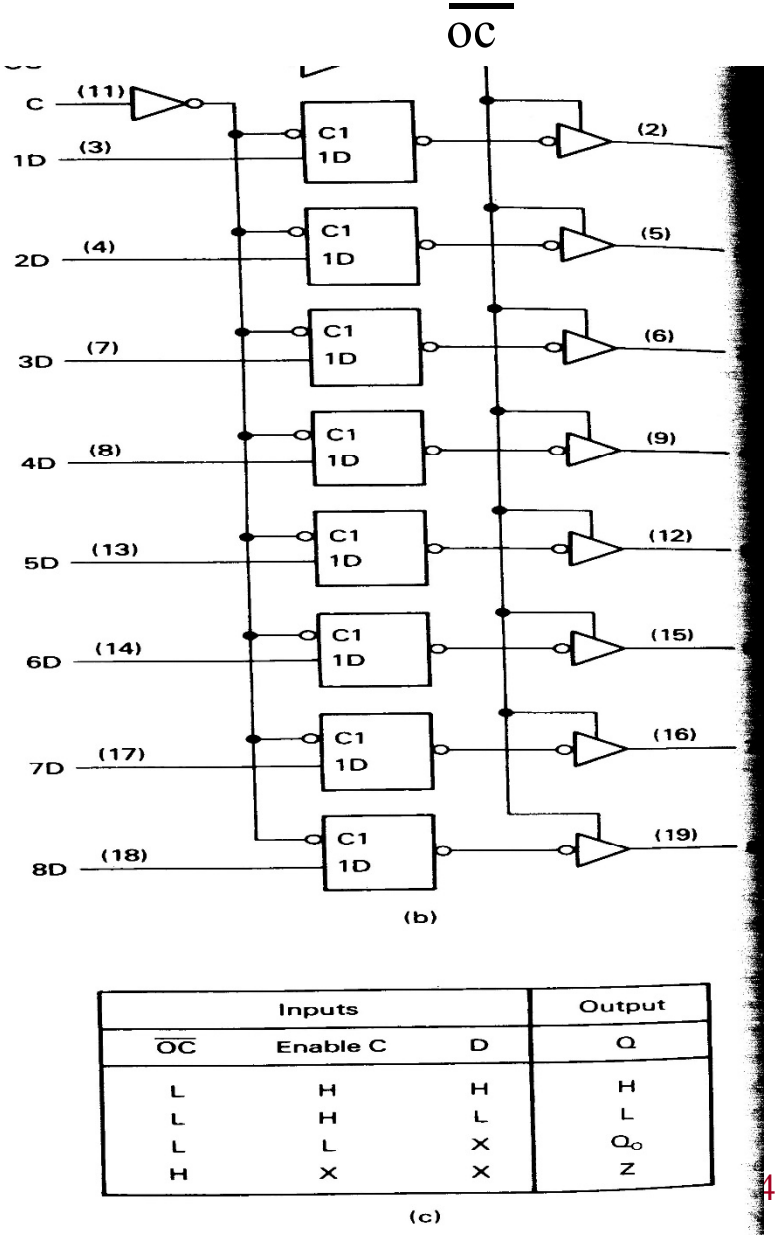
- BHE is output along with the address during T1
- Data can be read during T3 over all 16 data bus lines
- M/IO replaces IO/M
- SSO status signal is not produced



Address Bus Latches and Buffers



(a)

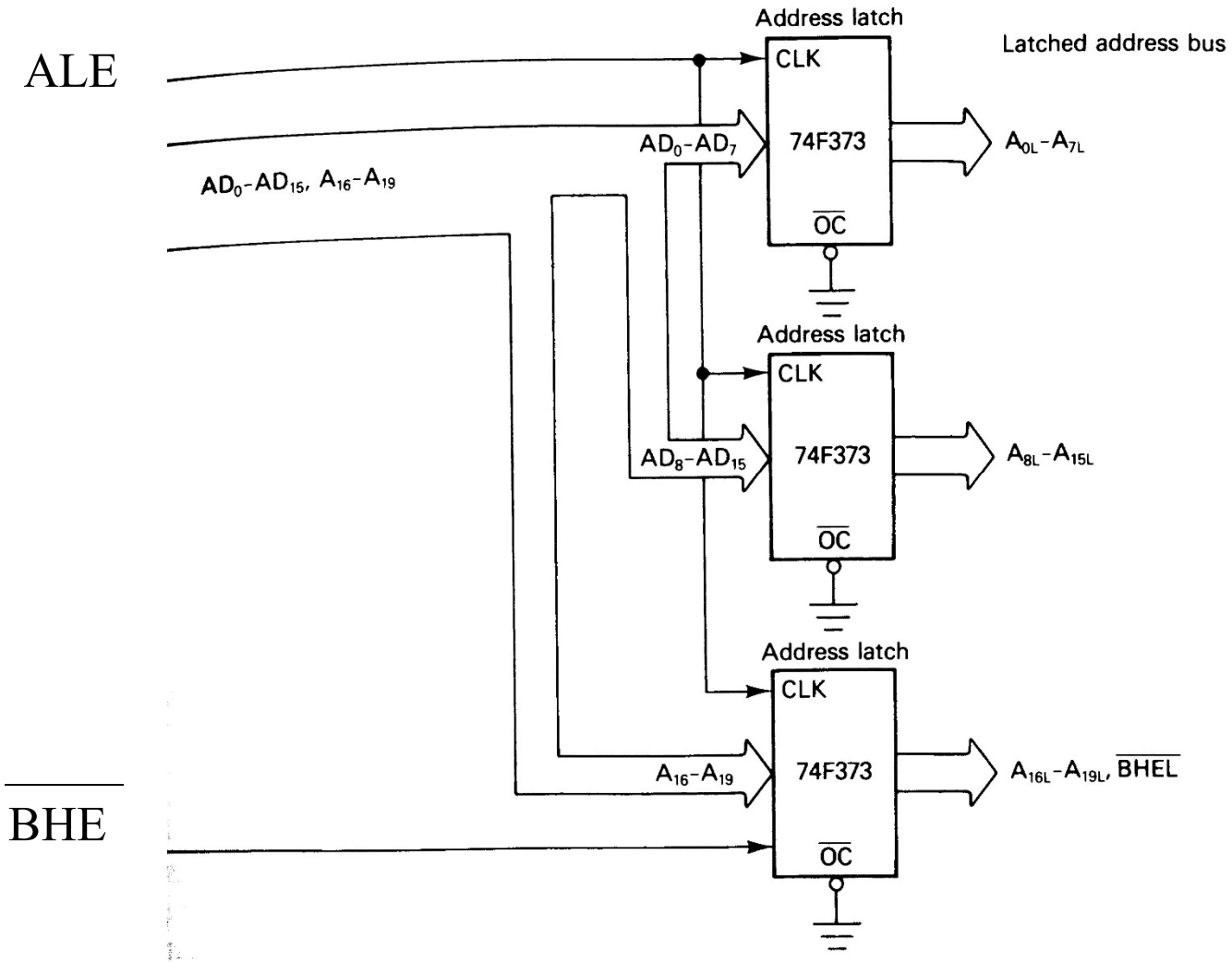


(b)

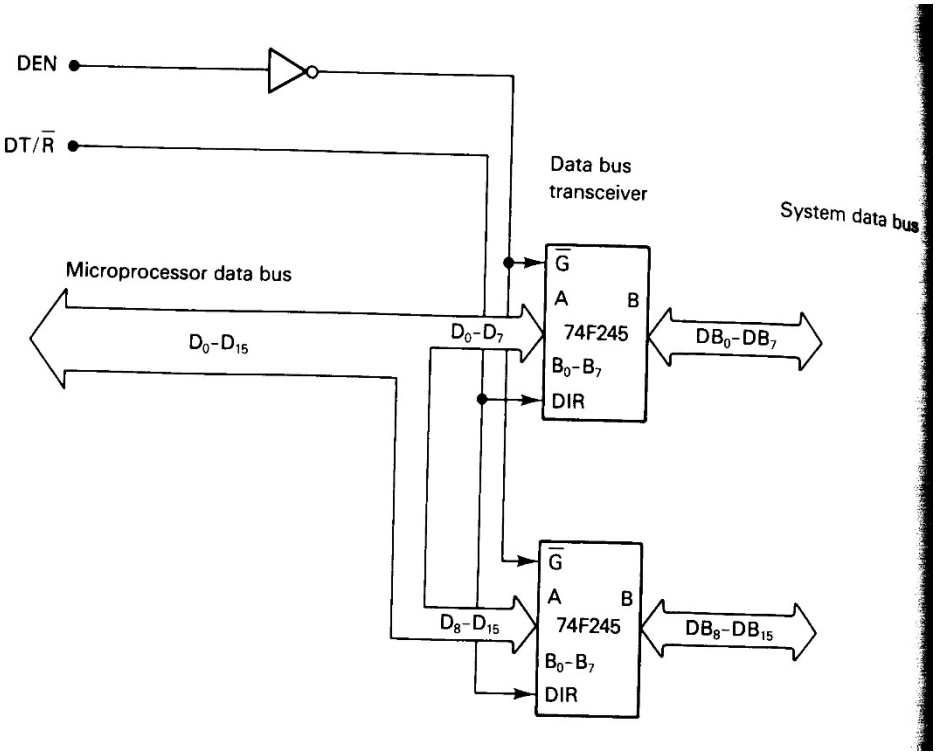
Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

(c)

Address Latch Circuit



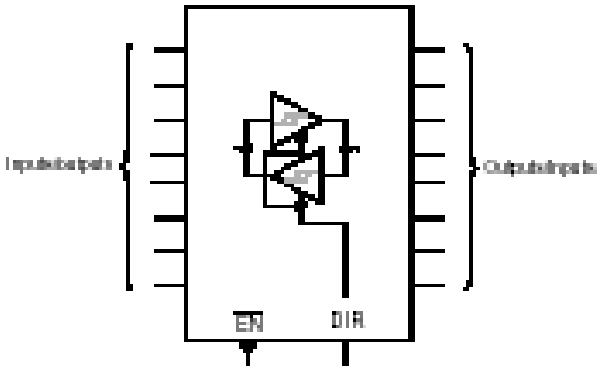
Data Bus Transceiver Circuit



GBAR ENABLE	DIR	OPERATION
L	L	B data to A
L	H	A data to B
H	x	Isolation

Buffered Systems

- Buffering (boosting) of the control, data, and address busses to provide sufficiently strong signals to drive various IC chips
  - When a pulse leaves an IC chip it can lose some of its strength depending on how far away the receiving IC is located
  - Plus the more pins a signal is connected to (i.e., fanout) the stronger the signal must be to drive them all which requires bus buffering
  - bus buffering = boosting the signals travelling on the busses
  - unidirectional bus 74LS244
  - bidirectional bus 74LS245



8088 System

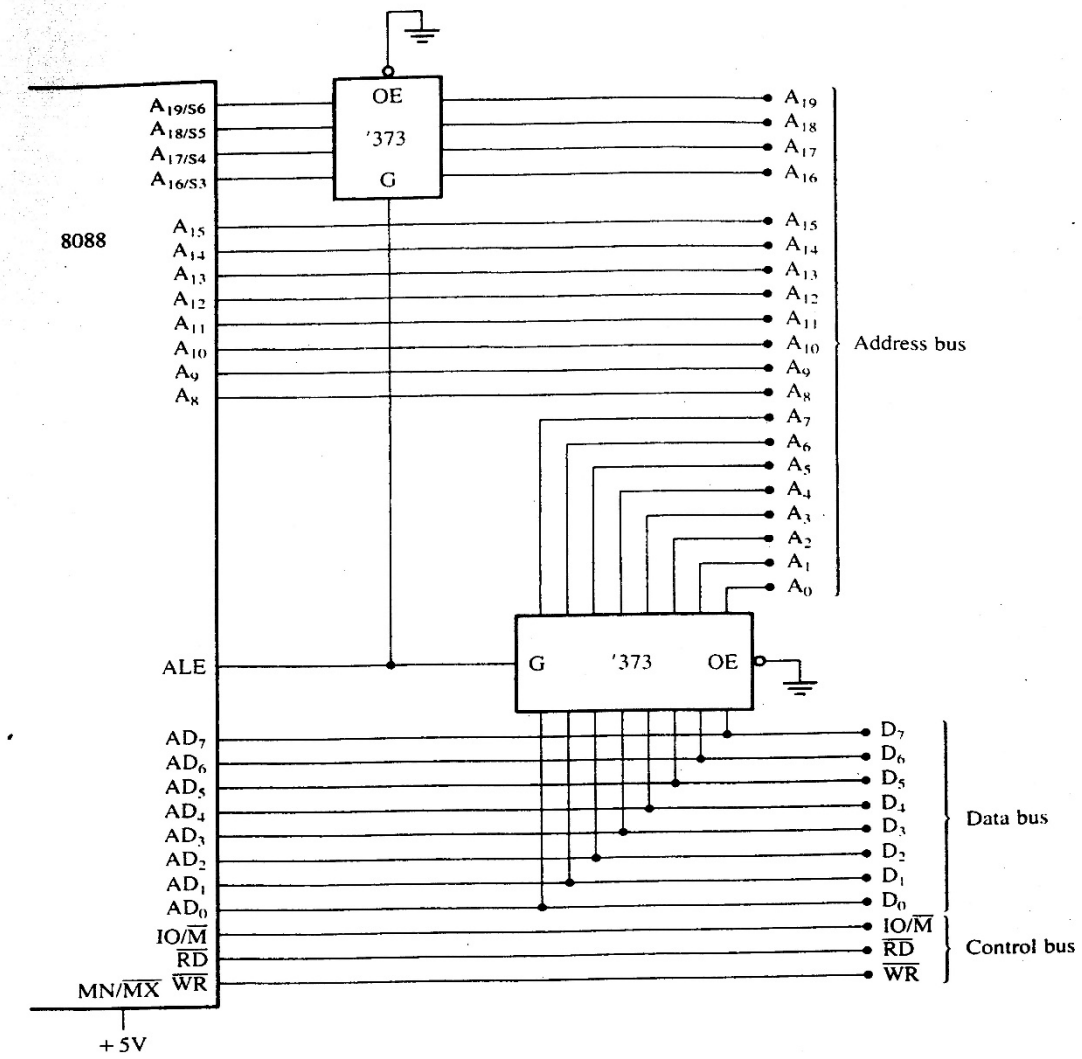
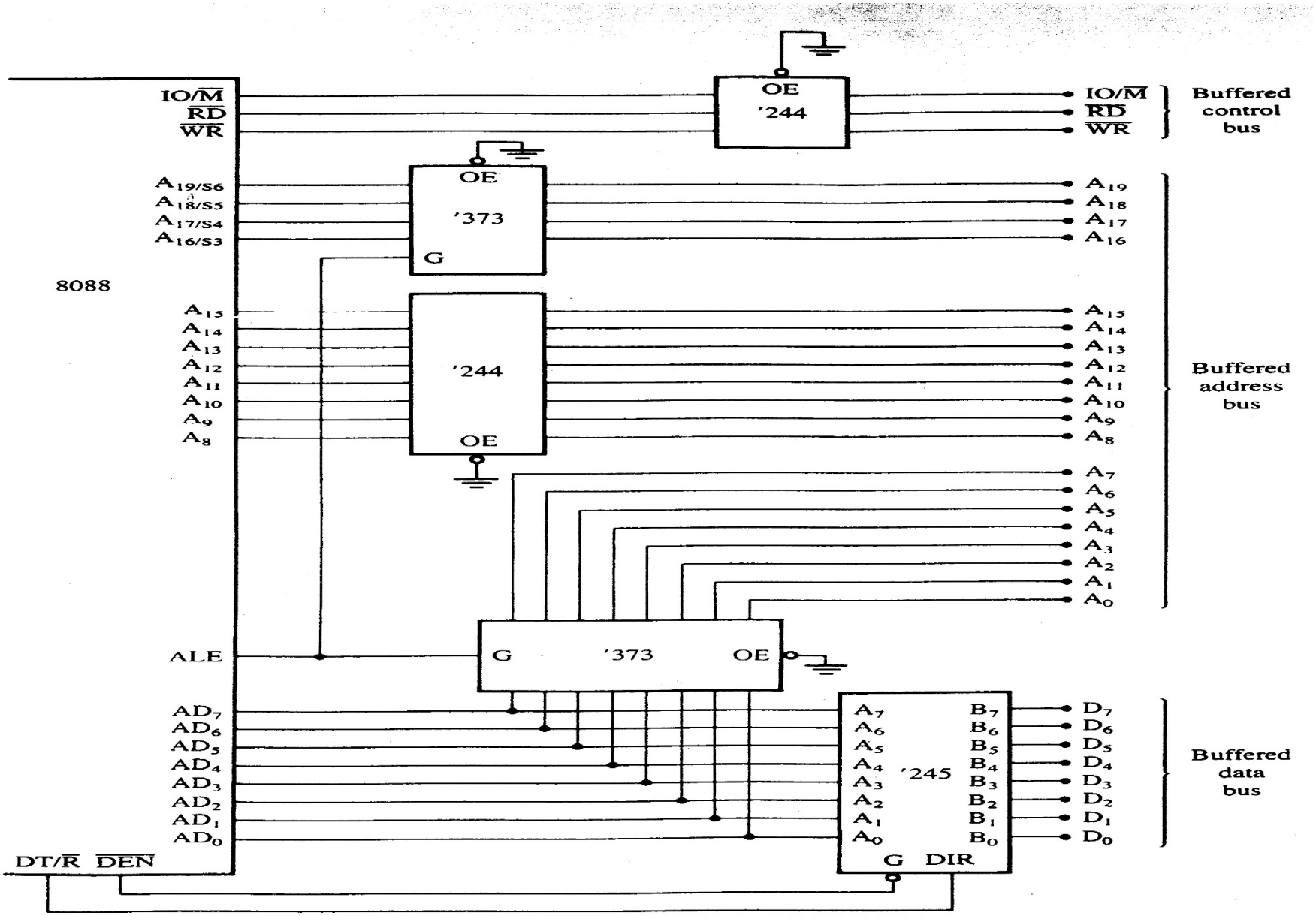
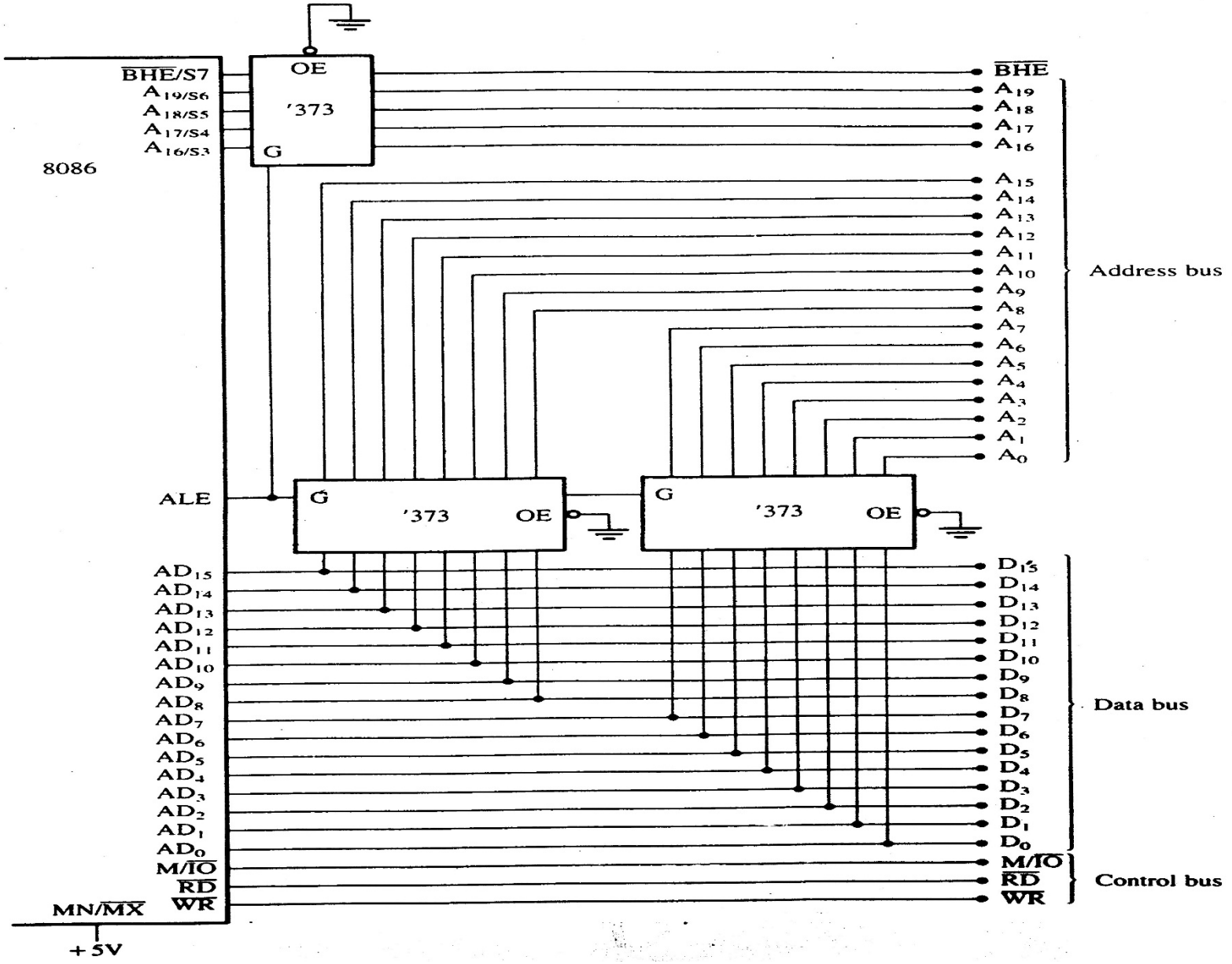


FIGURE 9–5 The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.

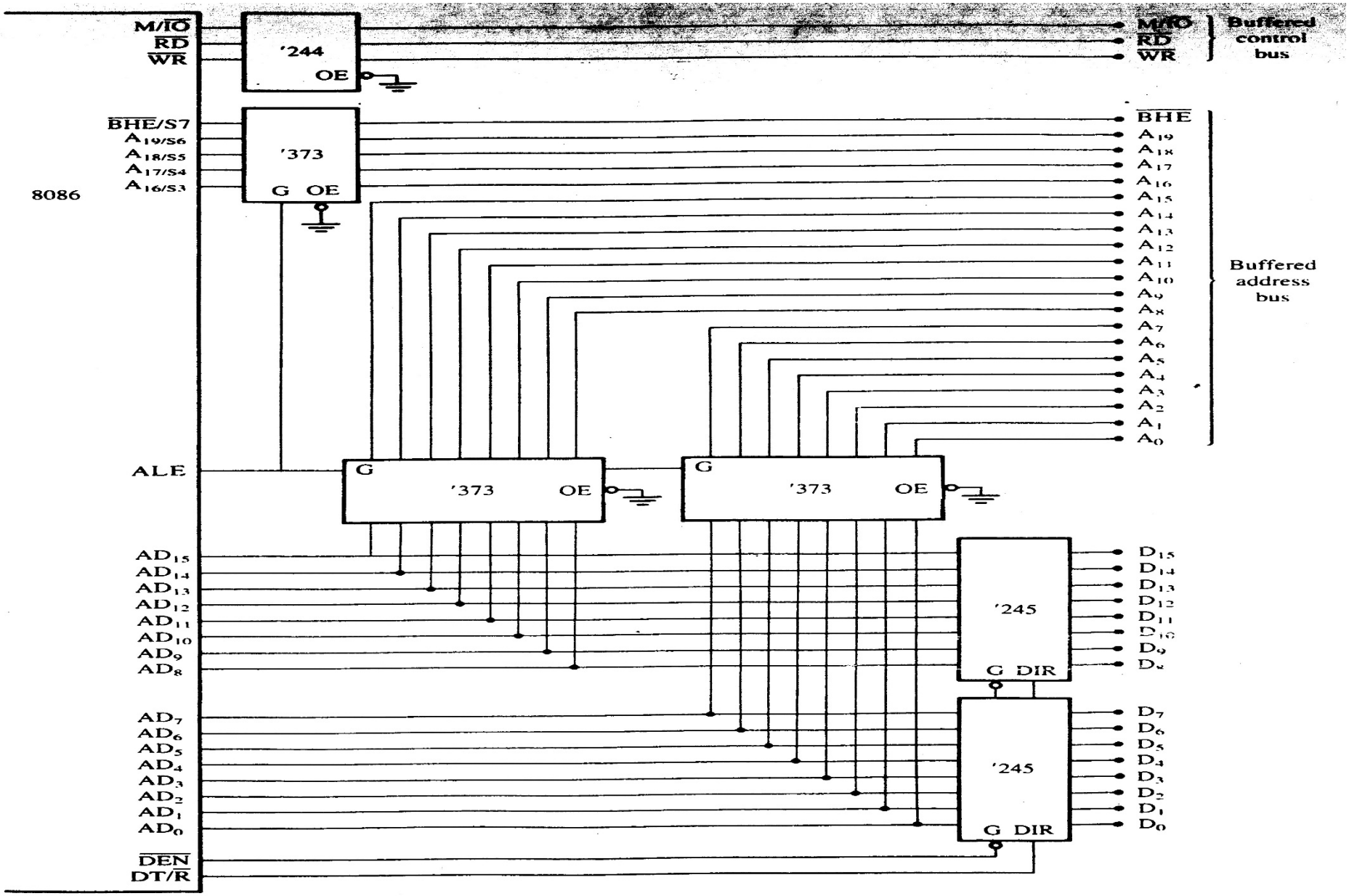
Fully buffered 8088



8086 System


8086
BHE/S7
A19/S6
A18/S5
A17/S4
A16/S3
OE
'373
G
BHE
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
Address bus
ALE
G
'373
OE
G
'373
OE
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
Data bus
M/IO
RD
WR
Control bus
MN/MX
+5V

Fully Buffered 8086



Memory Interface

- 8088 provides three pins for control signals:
  - RD, WR, and IO/M.
    - RD & WR pins are both *active-low*.
    - IO/M is *low* for memory, *high* for I/O devices.